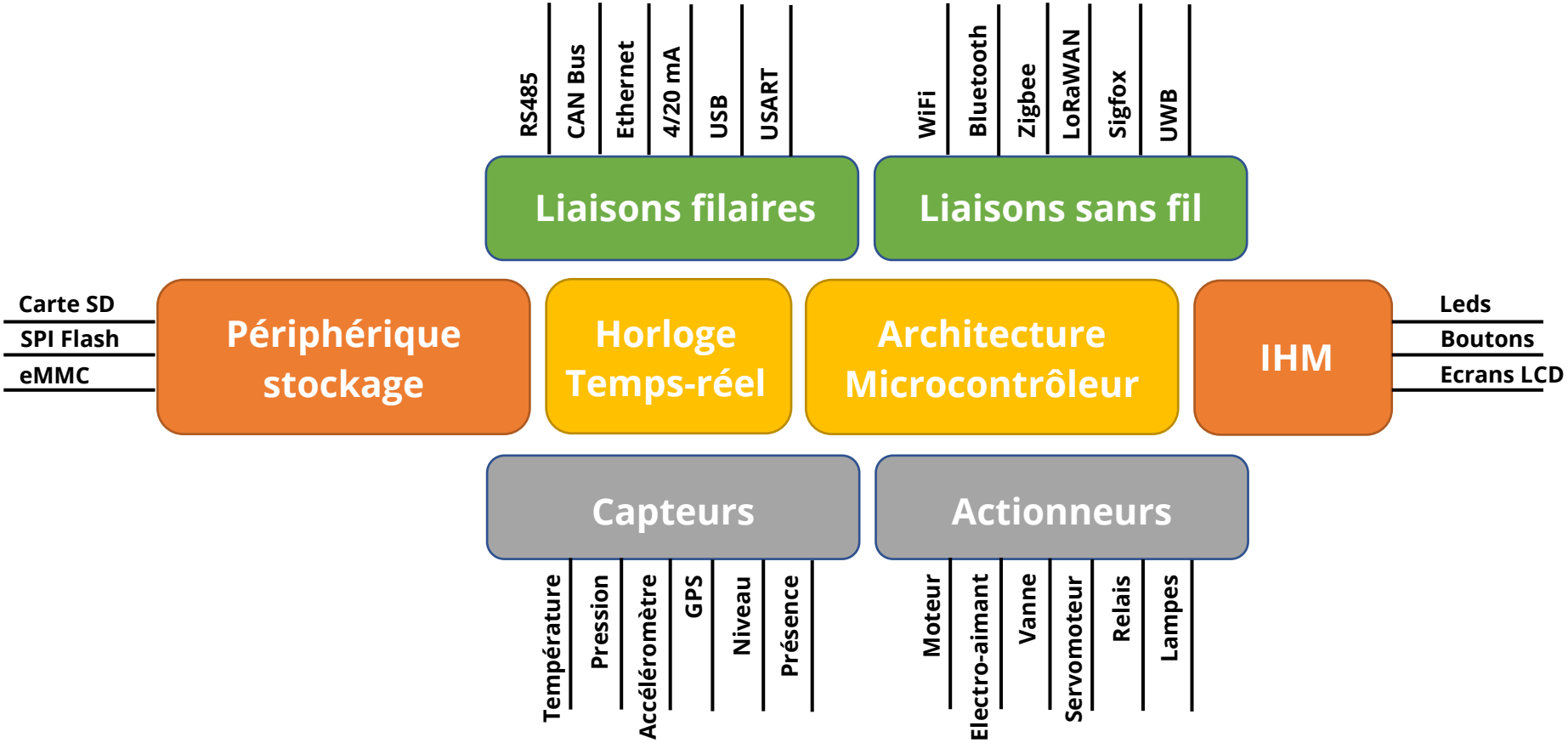
Partie 2

Acquisition des données

Systèmes embarqués pour l'IoT

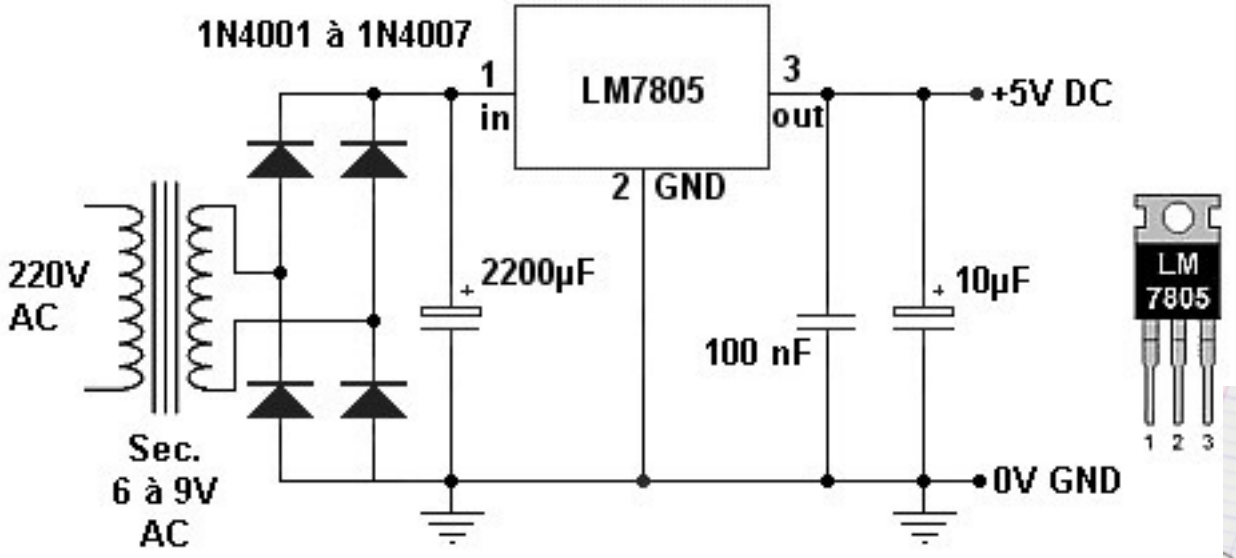
Modèle de système embarqué

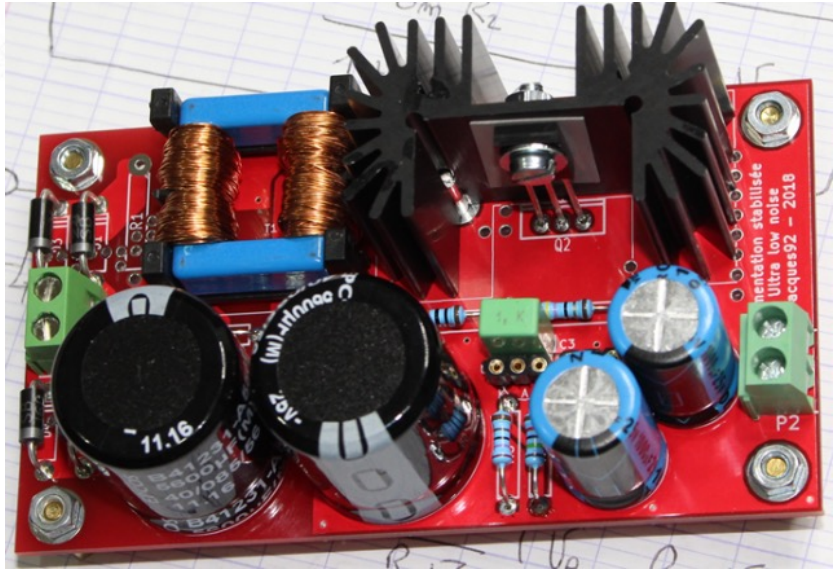


Mise en route d’un CPU

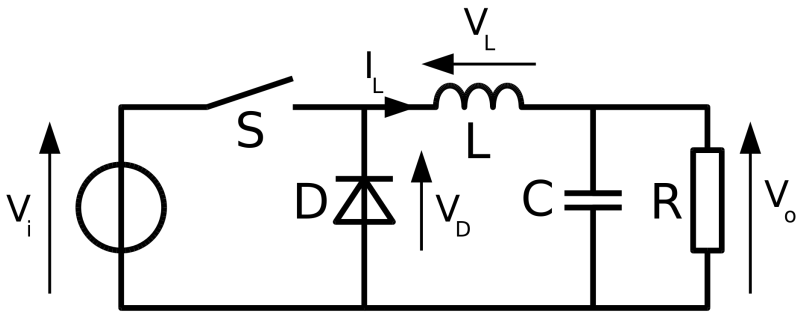
Alimentation, horloge numérique

Alimentation linéaire sur secteur

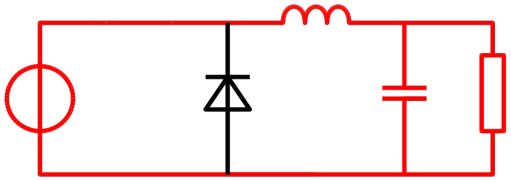




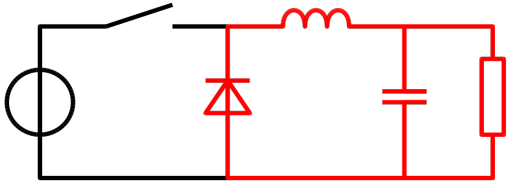
Alimentation à découpage

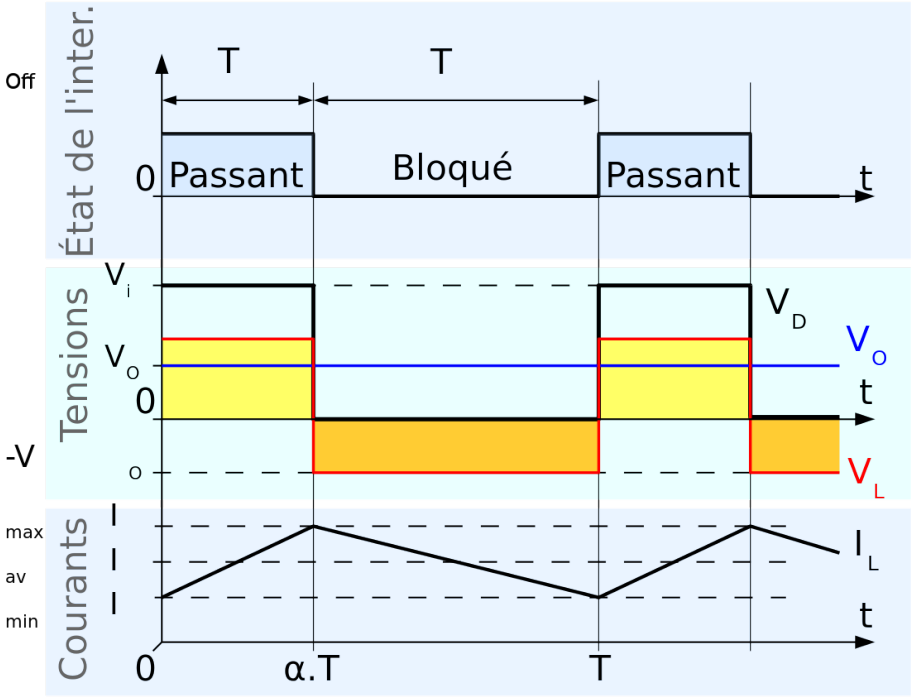


Interrupteur passant

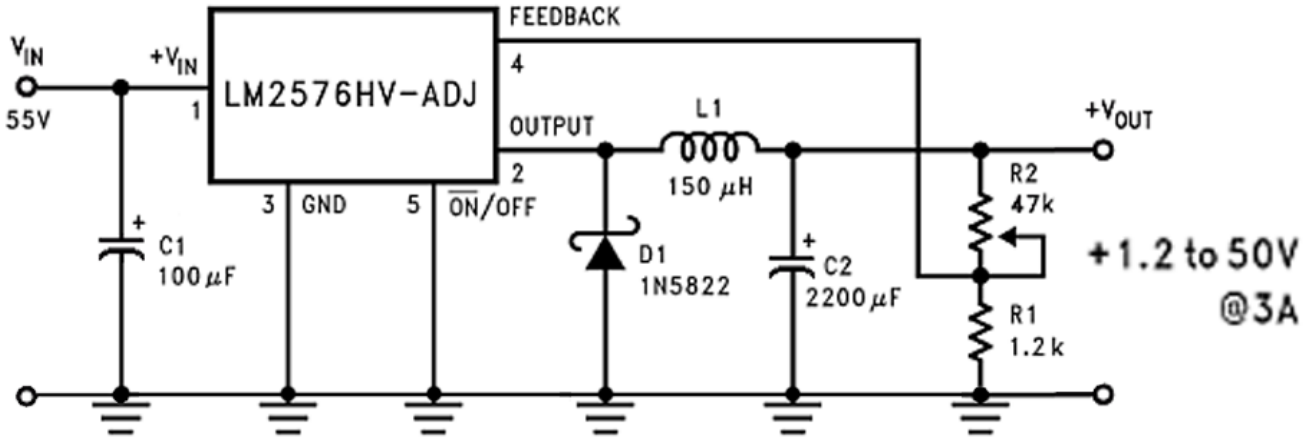


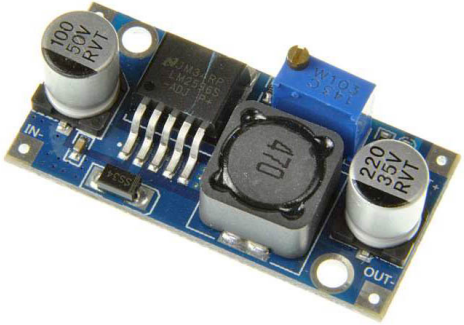
Interrupteur bloqué



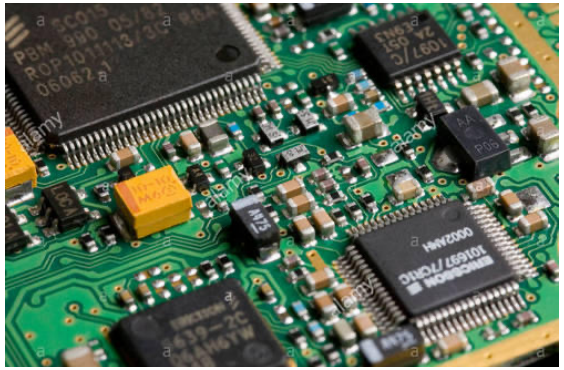


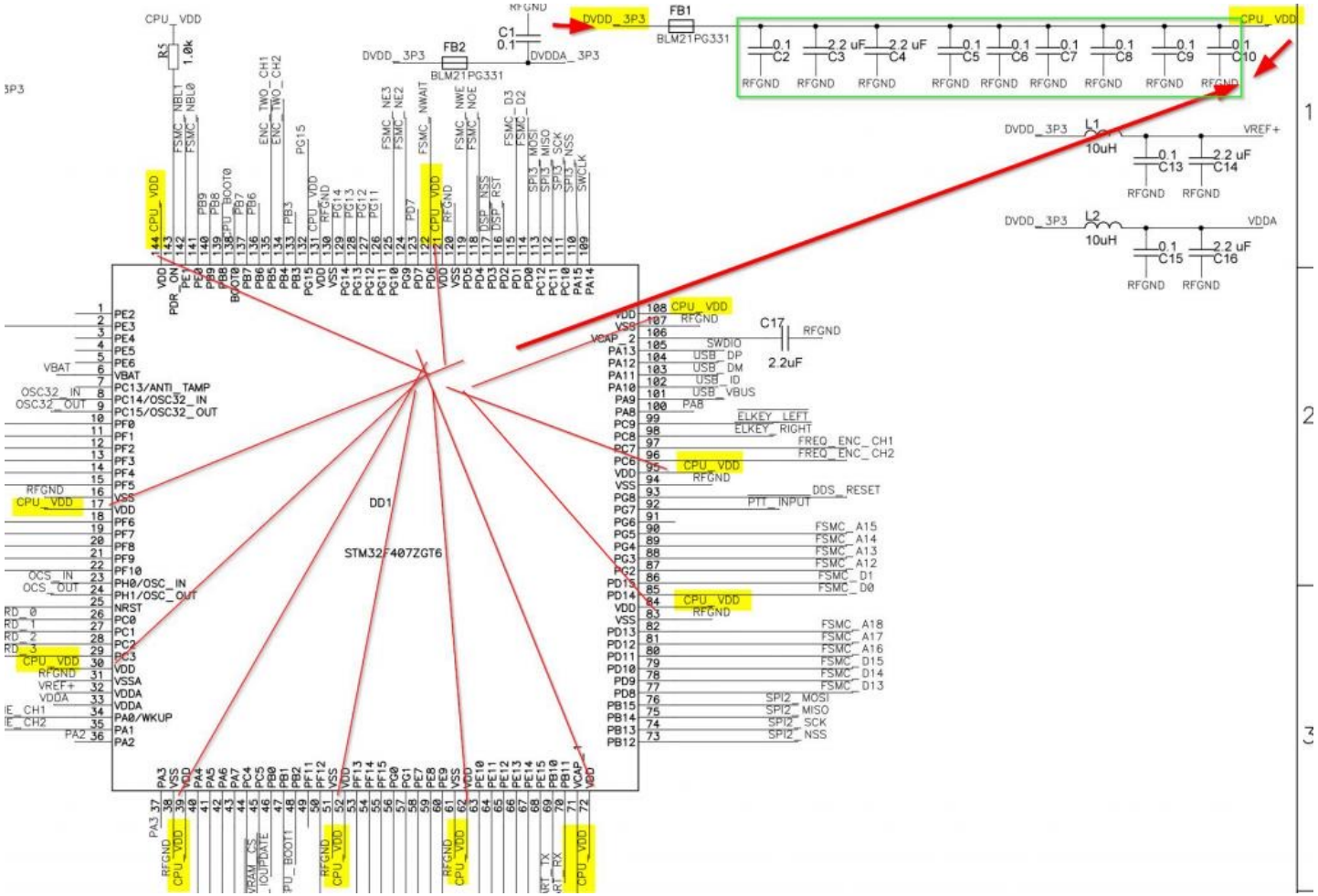
Alimentation à découpage



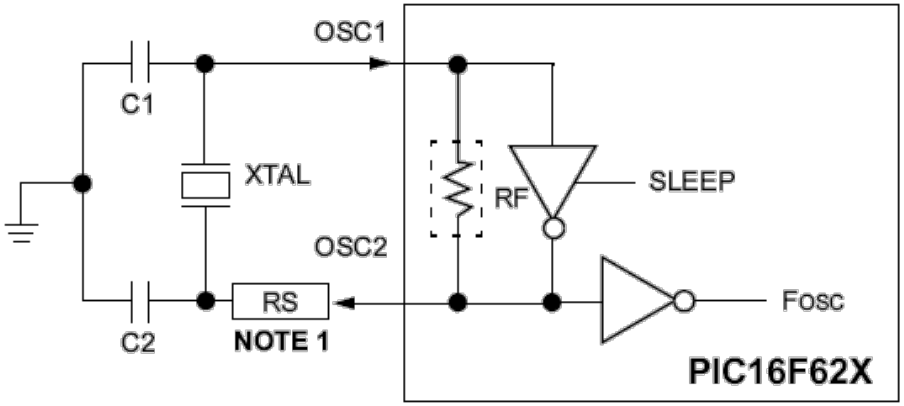


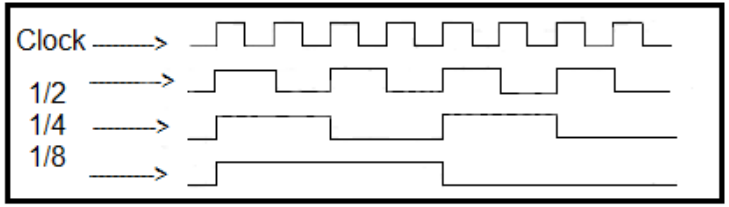
Condensateurs de découplage

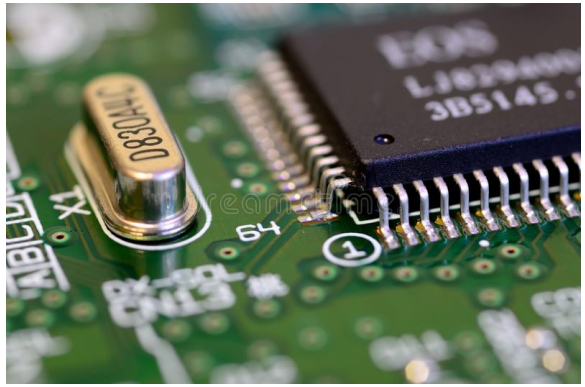




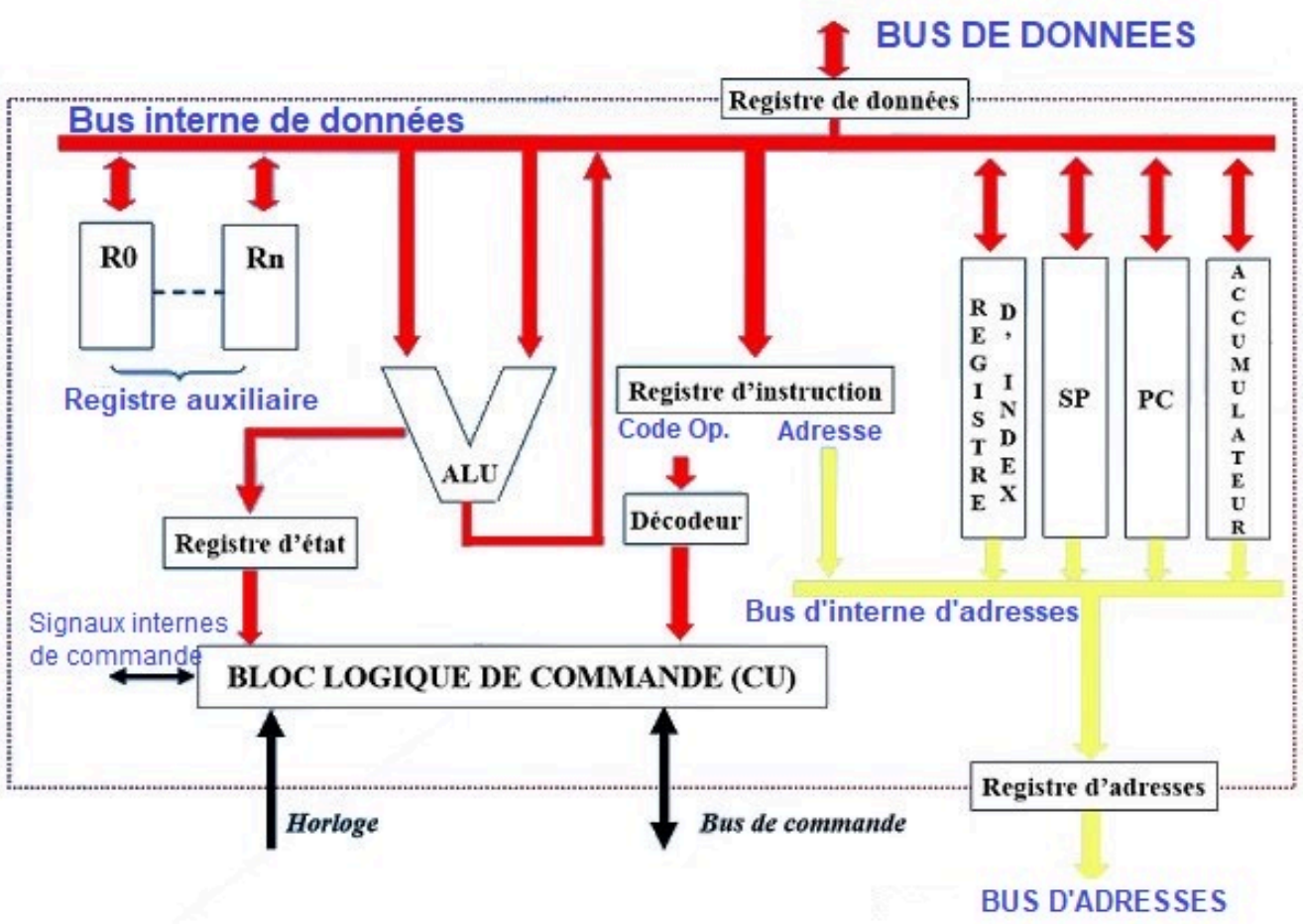
Génération d'horloge numérique







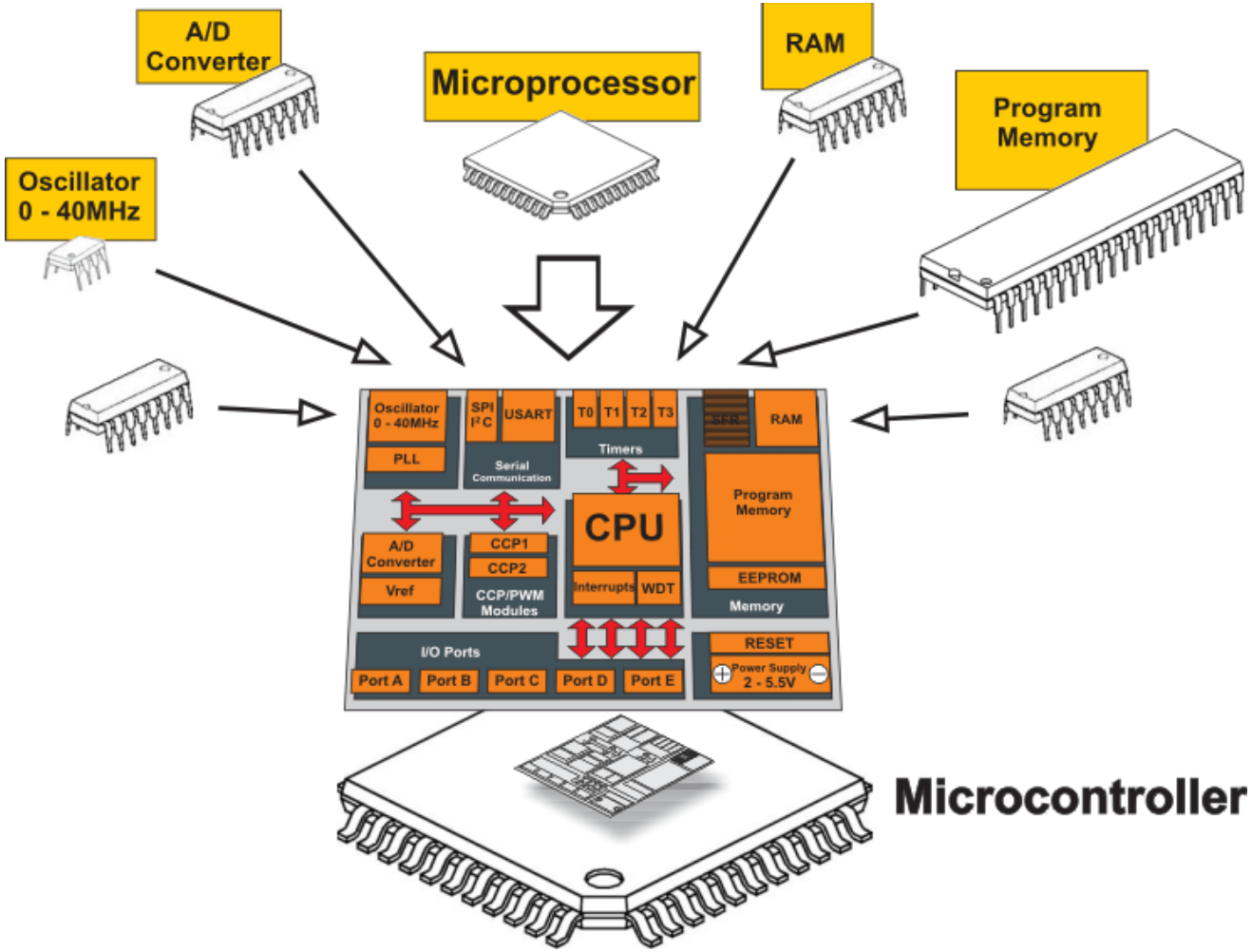
Unité arithmétique et logique



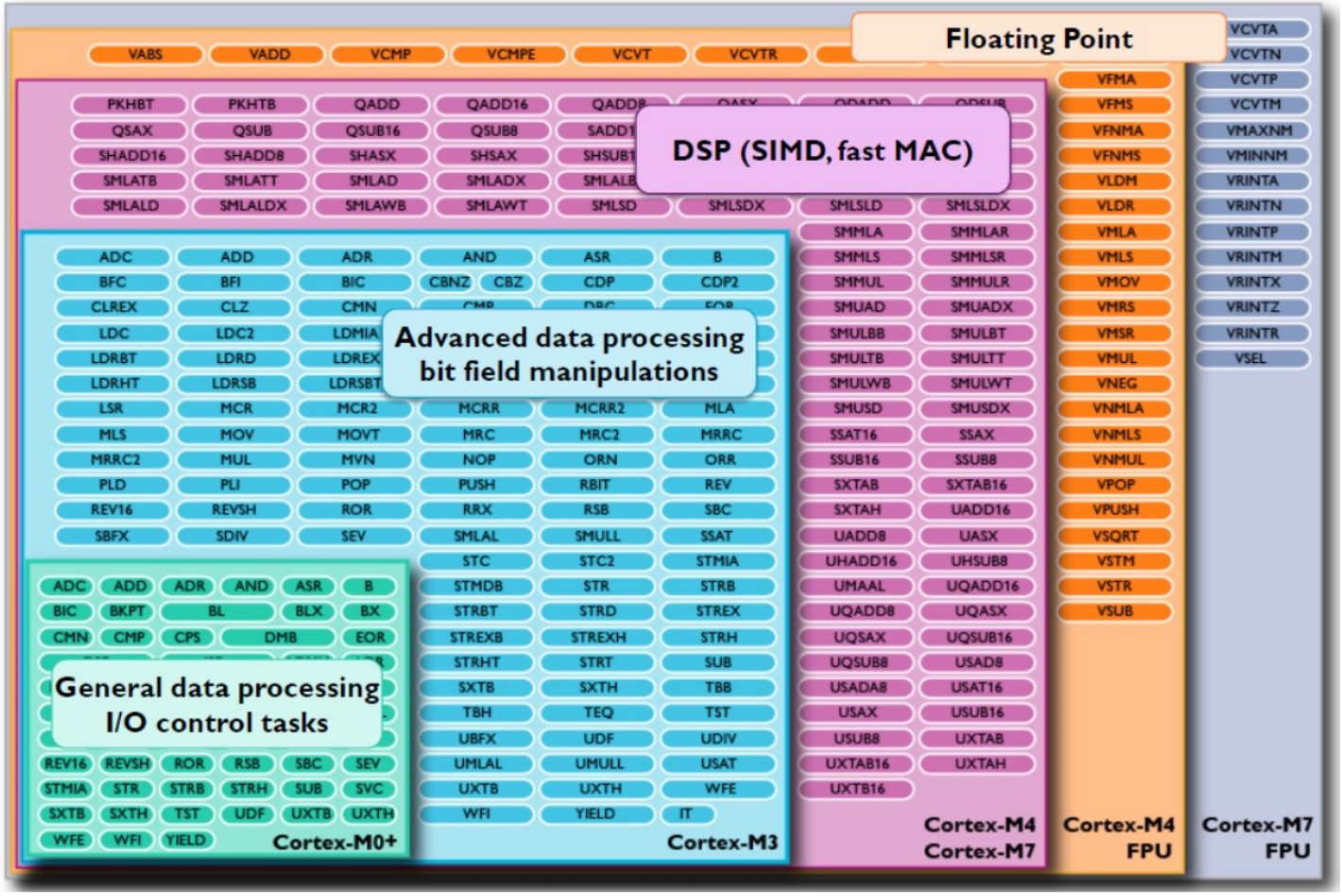
Systèmes embarqués

Les microcontrôleurs

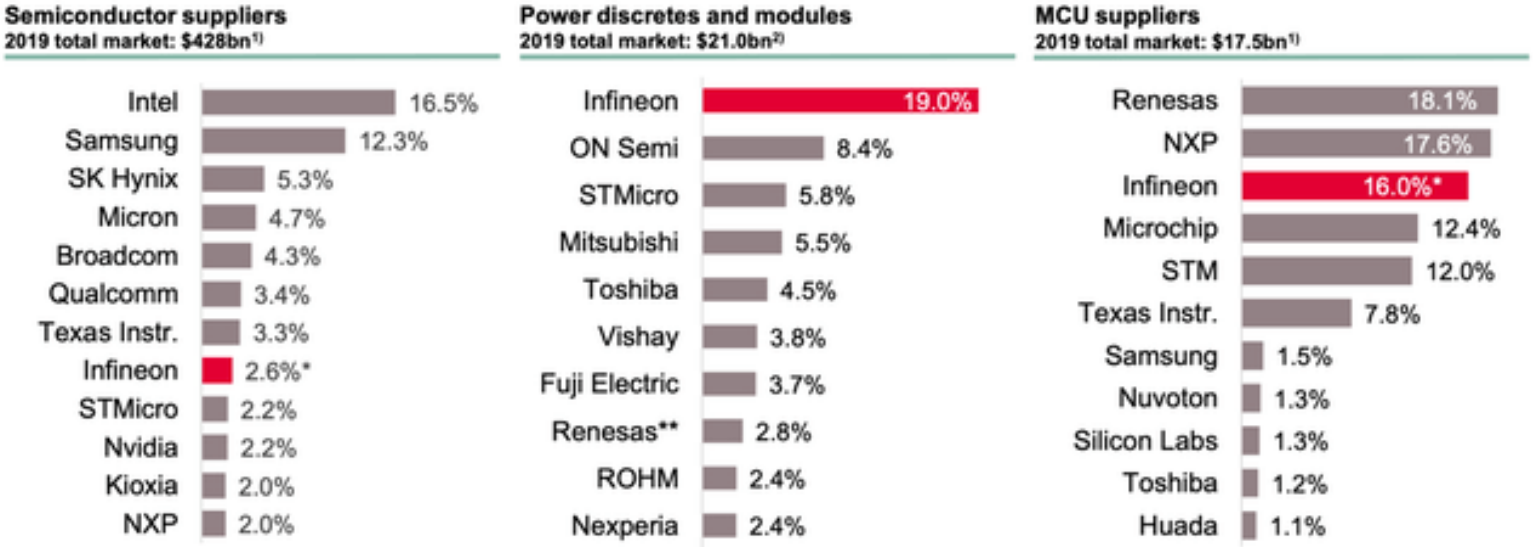
Microcontrôleur



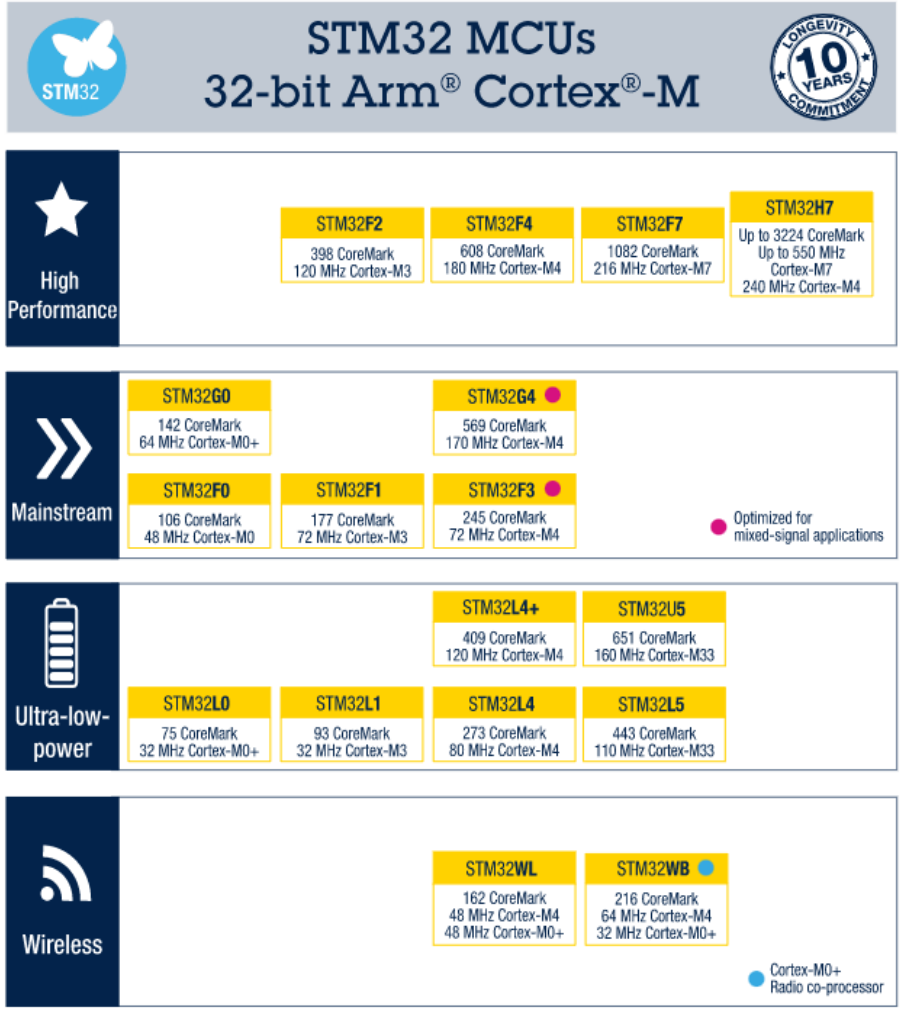
Modèle de l'architecture ARM



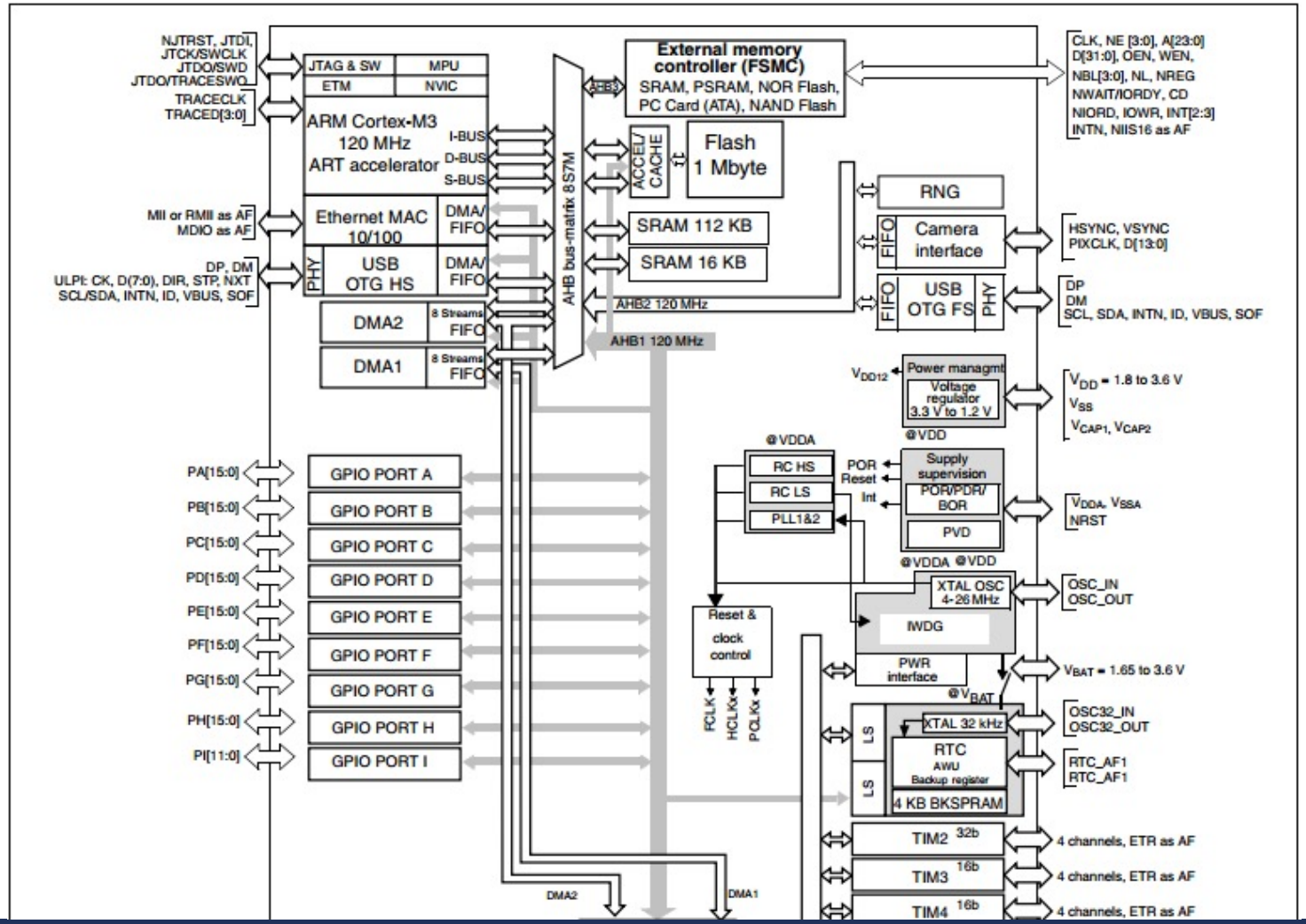
Constructeurs de Microcontrôleurs



STMicroelectronics



STM32


NJTRST, JTDI, JTCK/SWCLK JTDO/SWD JTDO/TRACESWO
TRACECLK TRACED[3:0]
JTAG & SW
MPU
ETM
NVIC
ARM Cortex-M3 120 MHz ART accelerator
I-BUS
D-BUS
S-BUS
MII or RMII as AF MDIO as AF
Ethernet MAC 10/100
DMA/ FIFO
DP, DM ULPI: CK, D(7:0), DIR, STP, NXT SCL/SDA, INTN, ID, VBUS, SOF
PHY
USB OTG HS
DMA/ FIFO
DMA2
8 Streams FIFO
DMA1
8 Streams FIFO
AHB bus-matrix 8S7M
AHB3
External memory controller (FSMC)
SRAM, PSRAM, NOR Flash, PC Card (ATA), NAND Flash
CLK, NE [3:0], A[23:0] D[31:0], OEN, WEN, NBL[3:0], NL, NREG NWAIT/IORDY, CD NIORD, IOWR, INT[2:3] INTN, NIIS16 as AF
ACCEL/ CACHE
Flash 1 Mbyte
SRAM 112 KB
SRAM 16 KB
AHB2 120 MHz
AHB1 120 MHz
RNG
FIFO
Camera interface
HSYNC, VSYNC PIXCLK, D[13:0]
FIFO
USB OTG FS
PHY
DP DM SCL, SDA, INTN, ID, VBUS, SOF
VDD12
Power managmt
Voltage regulator 3.3 V to 1.2 V
@VDD
VDD = 1.8 to 3.6 V
VSS
VCAP1, VCAP2
@VDDA
RC HS
RC LS
PLL1&2
POR Reset
Int
Supply supervision
POR/PDR/ BOR
PVD
@VDDA @VDD
VDDA, VSSA
NRST
PA[15:0]
PB[15:0]
PC[15:0]
PD[15:0]
PE[15:0]
PF[15:0]
PG[15:0]
PH[15:0]
PI[11:0]
GPIO PORT A
GPIO PORT B
GPIO PORT C
GPIO PORT D
GPIO PORT E
GPIO PORT F
GPIO PORT G
GPIO PORT H
GPIO PORT I
Reset & clock control
FCLK
HCLKx
PCLKx
XTAL OSC 4-26 MHz
OSC_IN OSC_OUT
IWDG
PWR interface
VBAT = 1.65 to 3.6 V
@VBAT
LS
XTAL 32 kHz
OSC32_IN OSC32_OUT
RTC
AWU
Backup register
RTC_AF1 RTC_AF1
4 KB BKSPRAM
TIM2 32b
4 channels, ETR as AF
TIM3 16b
4 channels, ETR as AF
TIM4 16b
4 channels, ETR as AF
DMA2
DMA1

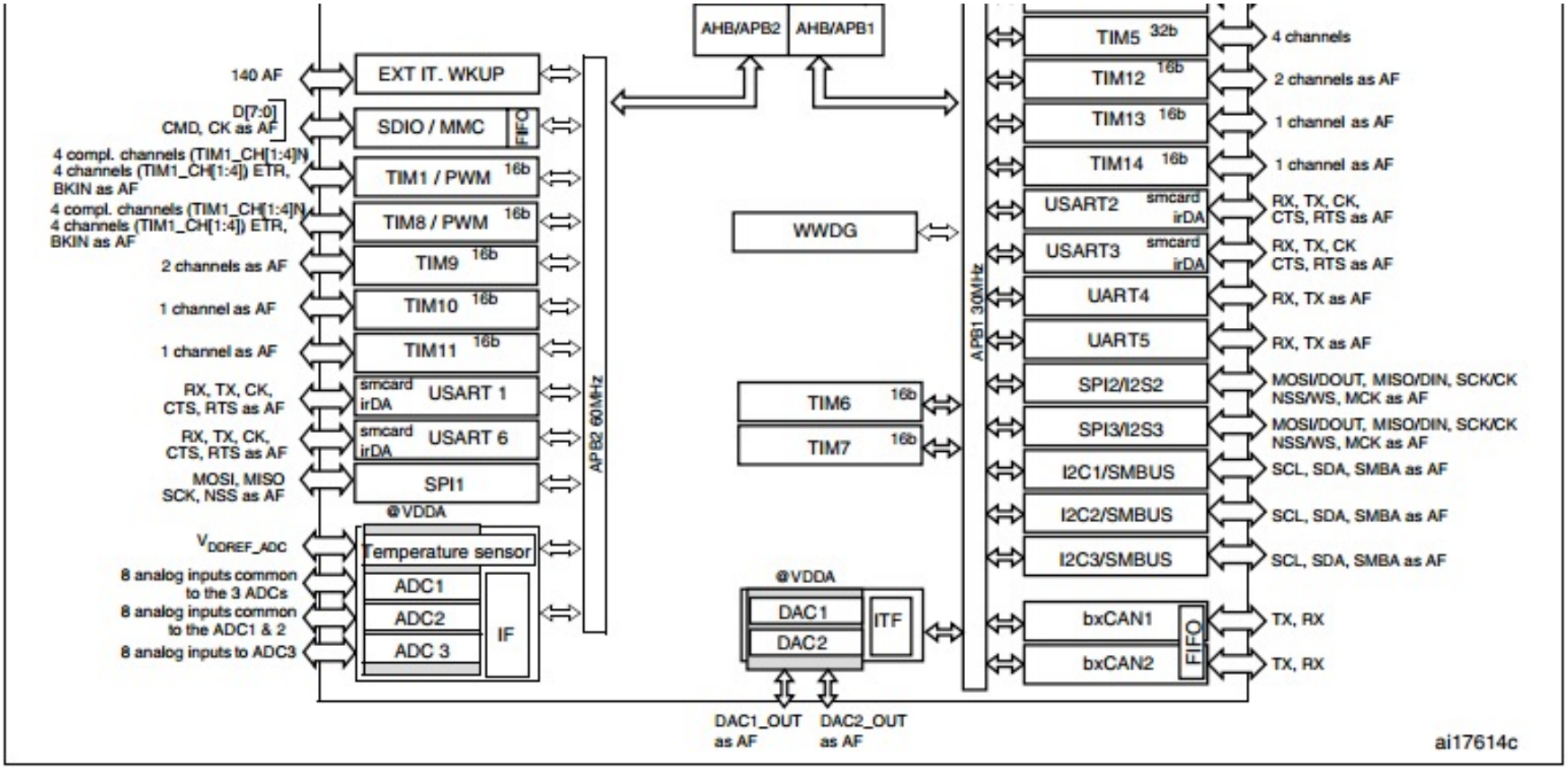

140 AF
EXT IT. WKUP
D[7:0]
CMD, CK as AF
SDIO / MMC
FIFO
4 compl. channels (TIM1_CH[1:4]N)
4 channels (TIM1_CH[1:4]) ETR,
BKIN as AF
TIM1 / PWM 16b
4 compl. channels (TIM1_CH[1:4]N)
4 channels (TIM1_CH[1:4]) ETR,
BKIN as AF
TIM8 / PWM 16b
2 channels as AF
TIM9 16b
1 channel as AF
TIM10 16b
1 channel as AF
TIM11 16b
RX, TX, CK,
CTS, RTS as AF
smcard irDA
USART 1
RX, TX, CK,
CTS, RTS as AF
smcard irDA
USART 6
MOSI, MISO
SCK, NSS as AF
SPI1
@VDDA
VDOREF_ADC
Temperature sensor
8 analog inputs common
to the 3 ADCs
ADC1
8 analog inputs common
to the ADC1 & 2
ADC2
8 analog inputs to ADC3
ADC 3
IF
APB2 60MHz
AHB/APB2
AHB/APB1
WWDG
TIM6 16b
TIM7 16b
@VDDA
DAC1
DAC2
ITF
DAC1_OUT
as AF
DAC2_OUT
as AF
APB1 30MHz
TIM5 32b
4 channels
TIM12 16b
2 channels as AF
TIM13 16b
1 channel as AF
TIM14 16b
1 channel as AF
USART2 smcard irDA
RX, TX, CK,
CTS, RTS as AF
USART3 smcard irDA
RX, TX, CK
CTS, RTS as AF
UART4
RX, TX as AF
UART5
RX, TX as AF
SPI2/I2S2
MOSI/DOUT, MISO/DIN, SCK/CK
NSS/WS, MCK as AF
SPI3/I2S3
MOSI/DOUT, MISO/DIN, SCK/CK
NSS/WS, MCK as AF
I2C1/SMBUS
SCL, SDA, SMBA as AF
I2C2/SMBUS
SCL, SDA, SMBA as AF
I2C3/SMBUS
SCL, SDA, SMBA as AF
bxCAN1
FIFO
TX, RX
bxCAN2
TX, RX
ai17614c

Table des registres

Table 14. Peripherals With Word Access

MODULE	REGISTER DESCRIPTION	REGISTER NAME	OFFSET
ADC10 (MSP430G2x53 devices only)	ADC data transfer start address	ADC10SA	1BCh
	ADC memory	ADC10MEM	1B4h
	ADC control register 1	ADC10CTL1	1B2h
	ADC control register 0	ADC10CTL0	1B0h
Timer1_A3	Capture/compare register	TA1CCR2	0196h
	Capture/compare register	TA1CCR1	0194h
	Capture/compare register	TA1CCR0	0192h
	Timer_A register	TA1R	0190h
	Capture/compare control	TA1CCTL2	0186h
	Capture/compare control	TA1CCTL1	0184h
	Capture/compare control	TA1CCTL0	0182h
	Timer_A control	TA1CTL	0180h
	Timer_A interrupt vector	TA1IV	011Eh
Timer0_A3	Capture/compare register	TA0CCR2	0176h
	Capture/compare register	TA0CCR1	0174h
	Capture/compare register	TA0CCR0	0172h
	Timer_A register	TA0R	0170h
	Capture/compare control	TA0CCTL2	0166h
	Capture/compare control	TA0CCTL1	0164h
	Capture/compare control	TA0CCTL0	0162h
	Timer_A control	TA0CTL	0160h
	Timer_A interrupt vector	TA0IV	012Eh
Flash Memory	Flash control 3	FCTL3	012Ch
	Flash control 2	FCTL2	012Ah
	Flash control 1	FCTL1	0128h
Watchdog Timer+	Watchdog/timer control	WDTCTL	0120h

M5STACK

ESPRESSIF
DevCon22

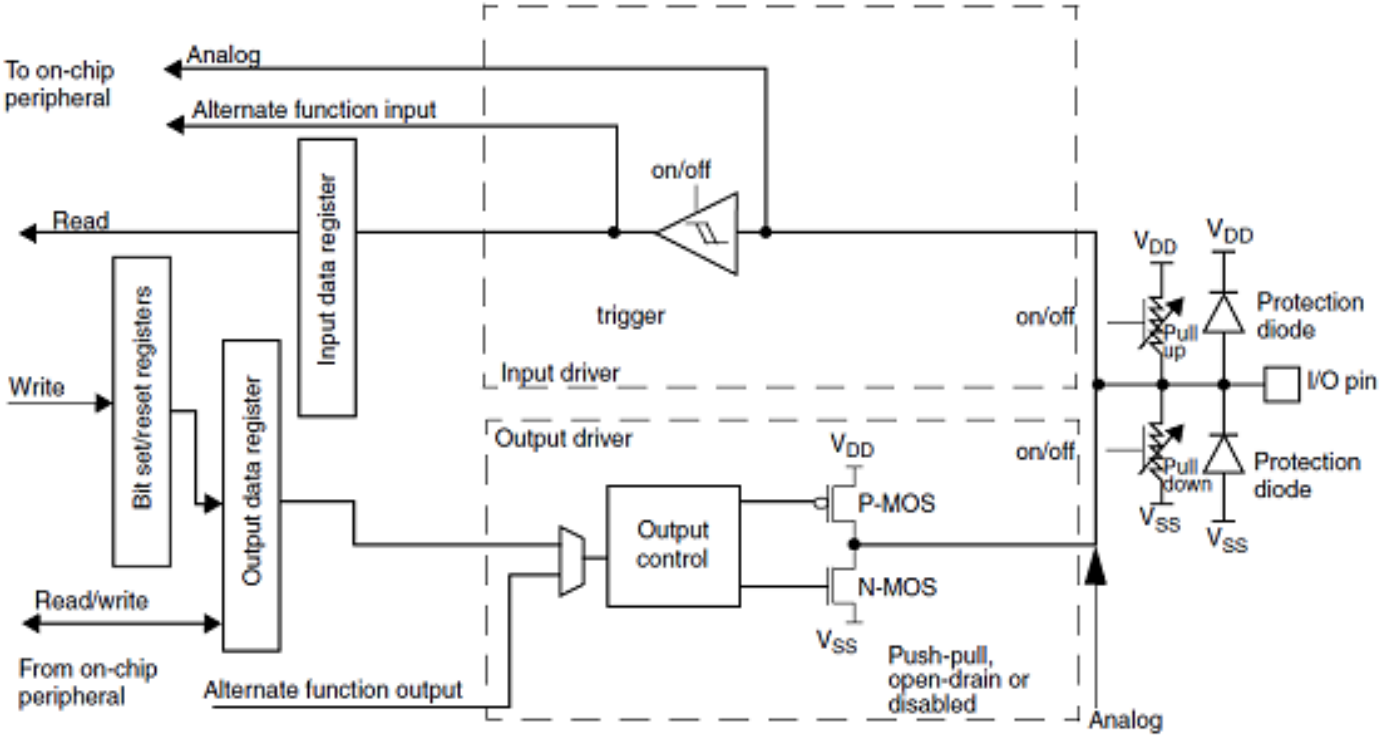
2X15 BUS
@2. 54mm
ESP32
3D-ANT
1W-SPEAKER
AUDIO-AMP
IP5306
EA3036
CP2014
RESET/
ON-OFF
BATTERY
SOCKET
TYPE-C
TF READER
GROVE
(I2C)

M5
CORE2 FOR AWS
ATECC608A
SECURE ELEMENT
M5STACK
POGO
PIN
(I2C)
RGB LED
SK6812
(G25)
MPU
6886
2"LCD
320*240
BATTERY
INSIDE
TOUCH
SCREEN
3mm
SCREW
HOLE
powered by
aws
PORT.C
ESP32
D0WDQ6-V3
16M-FLASH
8M-PSRAM
PWR
6s=OFF
AXP_PWR
PORT.B
RST
SYSTEM
USB-C
LED
PORT.A
PDM
MICROPHONE
TF
CARD
UIFlow
Arduino
FreeRTOS
MicroPython
54x54x24mm
CP2104
AXP192
MPU6886
RTC@BM8563
1W SPK@NS4168(I2S)
BATTERY: 3.7V/500mAh
2"LCD 320x240@ILI9342C
MICROPHONE@SPM1423
CAP.TOUCH/VIBRATION MOTOR

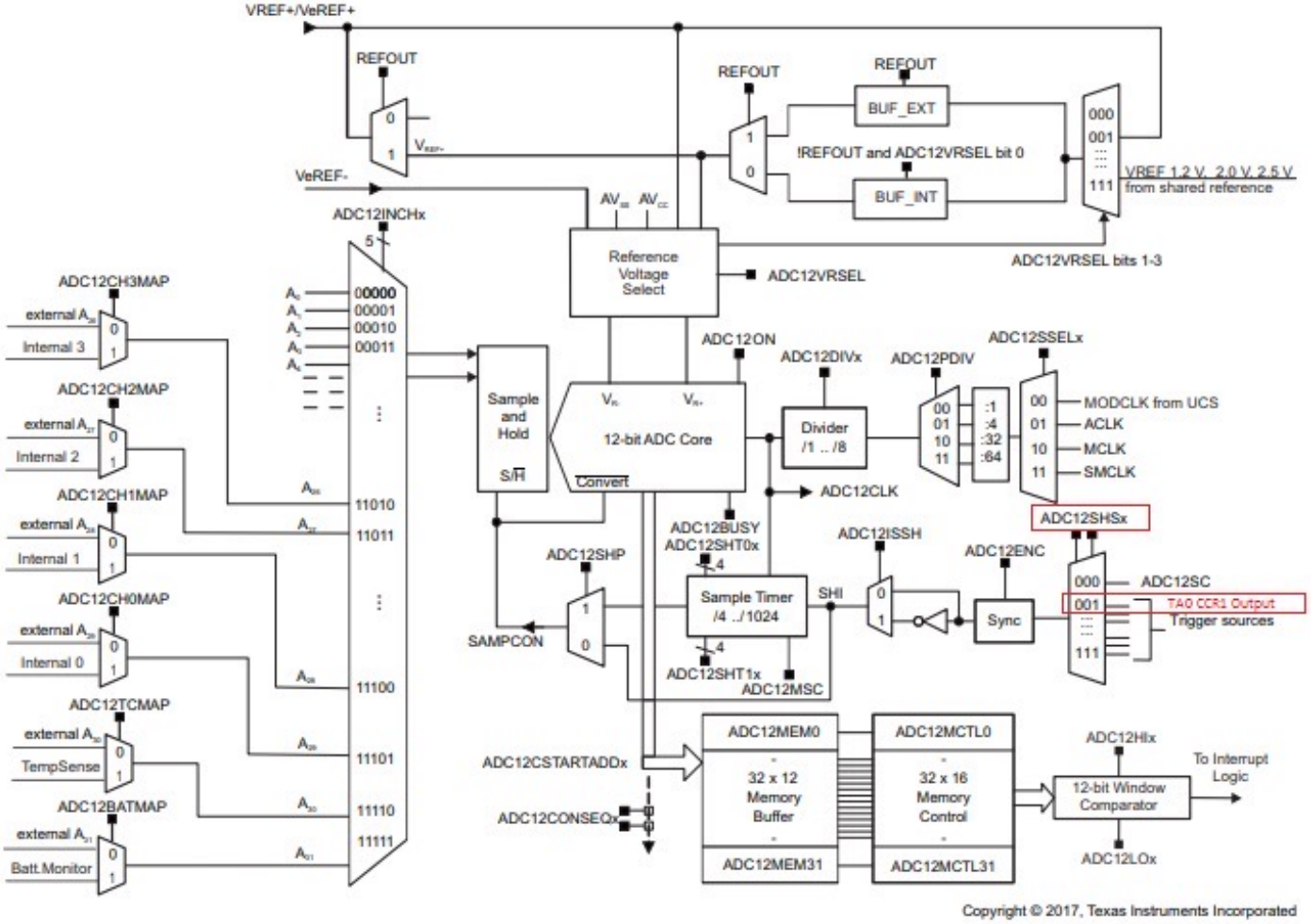
Entrées / Sorties

Conversion analogique <-> numérique

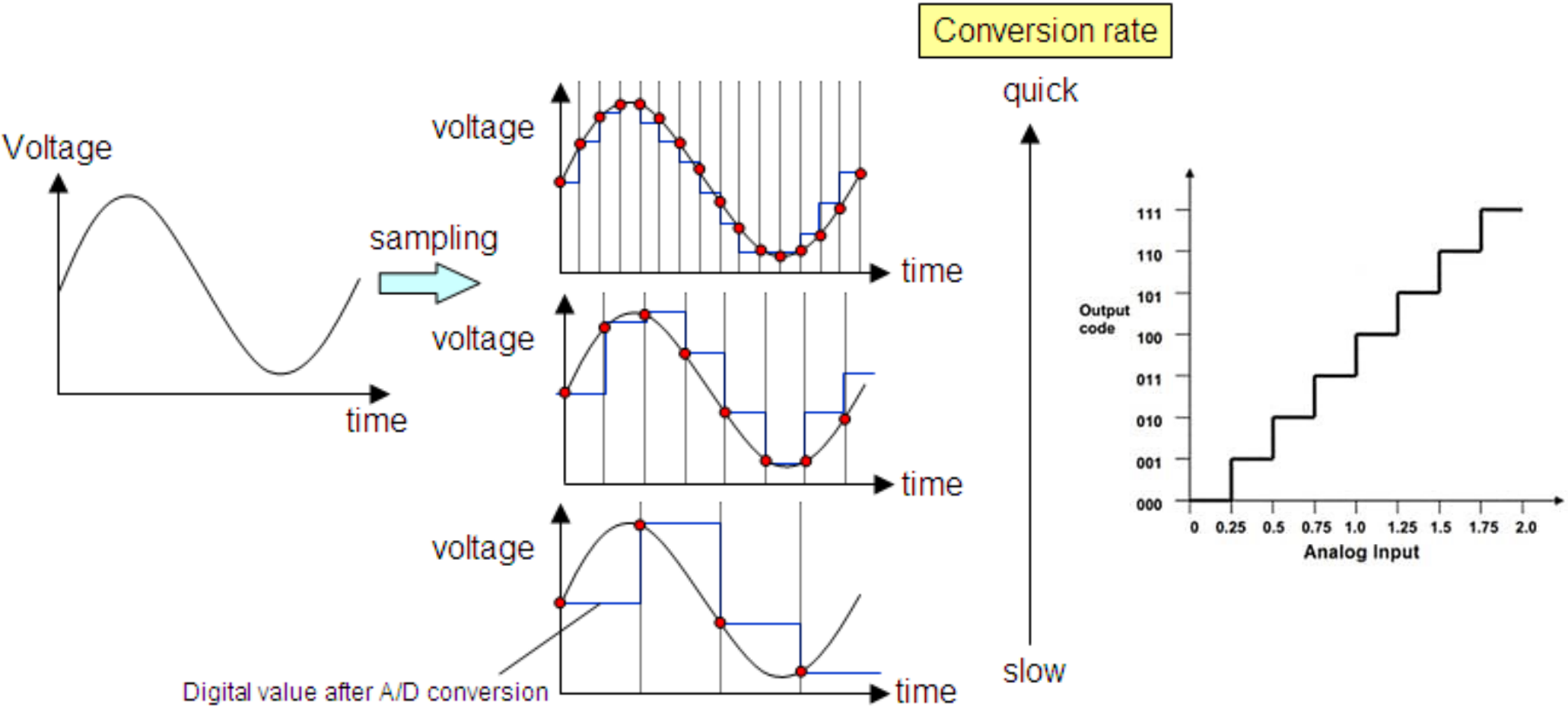
General Purpose Input/Output (GPIO)



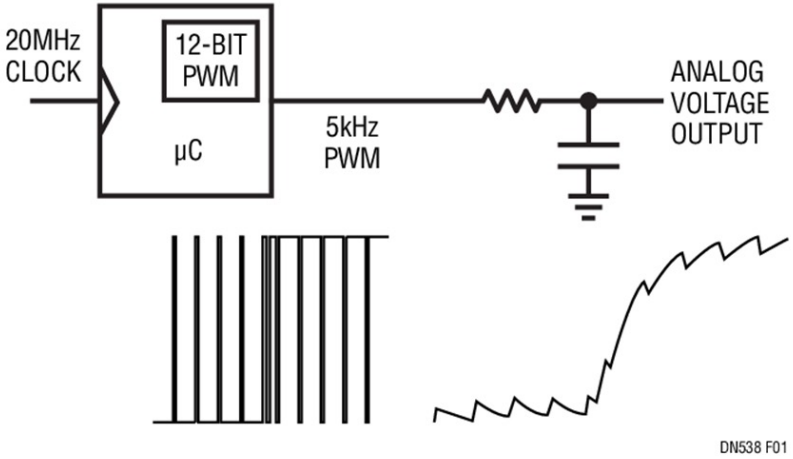
Convertisseur analogique / numérique

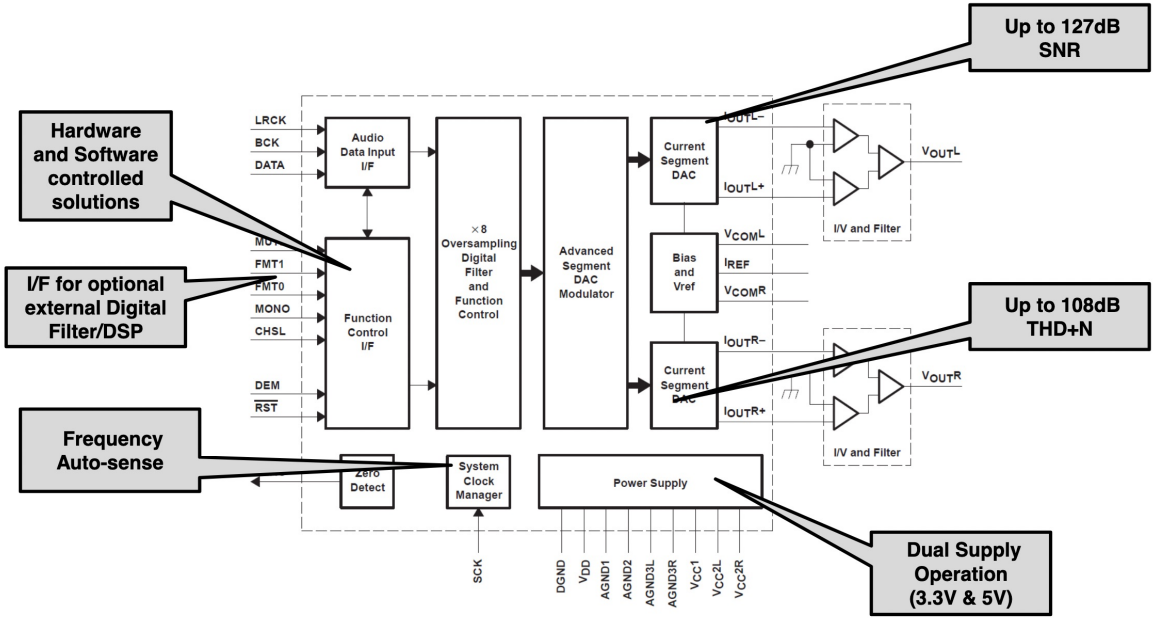


Convertisseur analogique / numérique

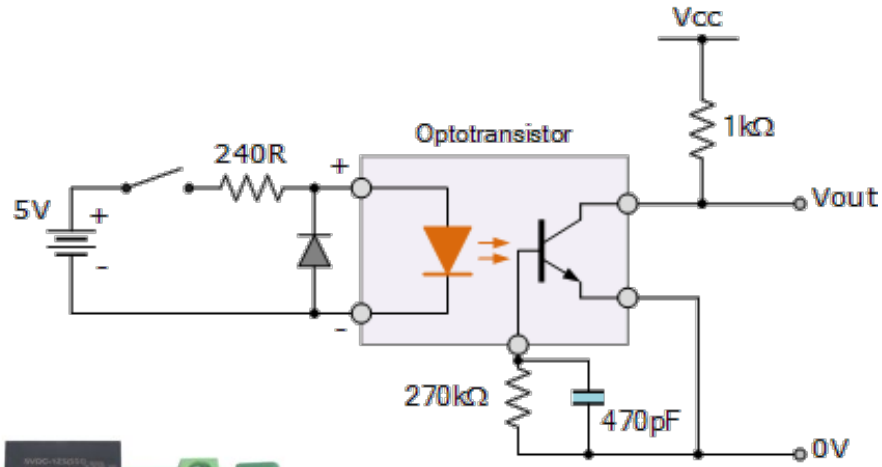


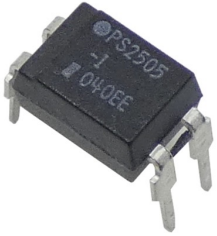
Convertisseur numérique / analogique





Isolation galvanique

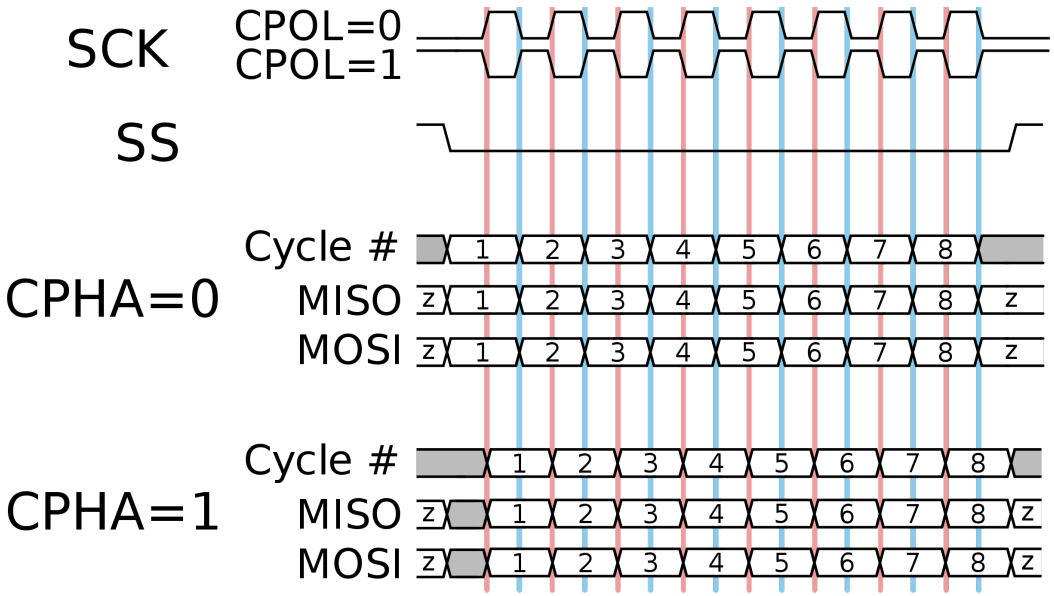


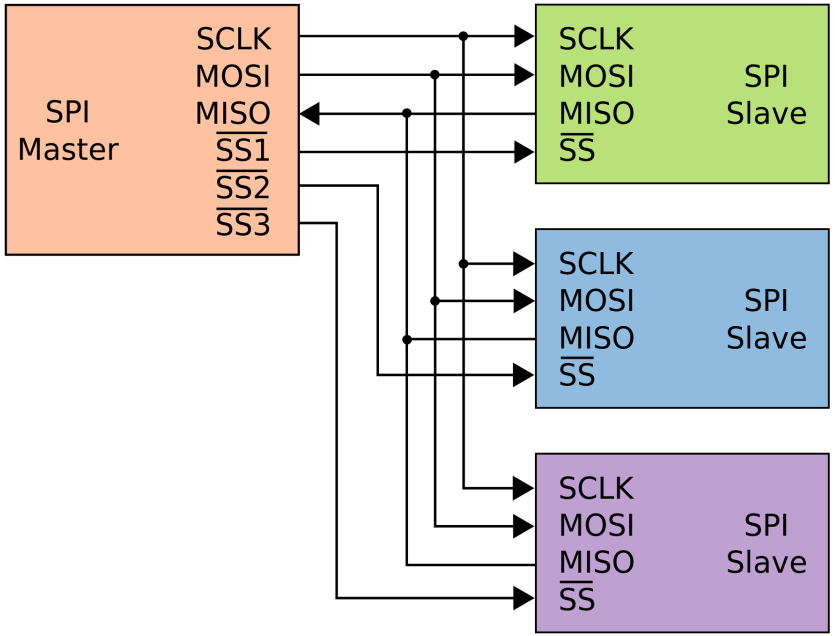


Bus de communication

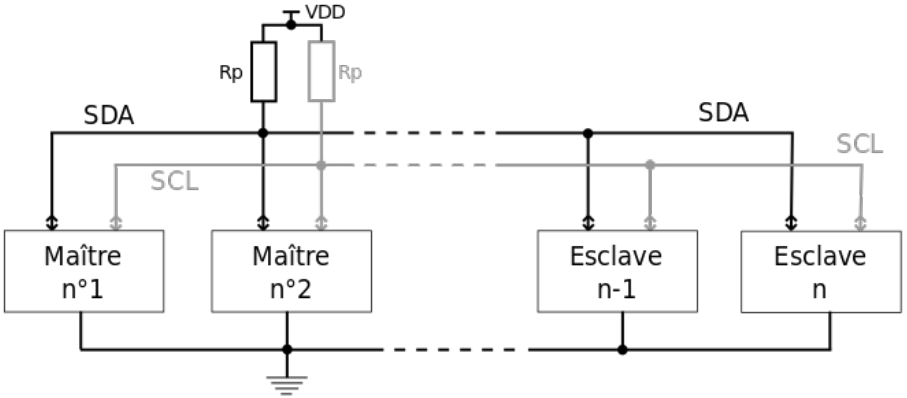
I2C, SPI, UART, Bus CAN, RS486

SPI


SCK
CPOL=0
CPOL=1
SS
CPHA=0
Cycle #
MISO
MOSI
CPHA=1
Cycle #
MISO
MOSI

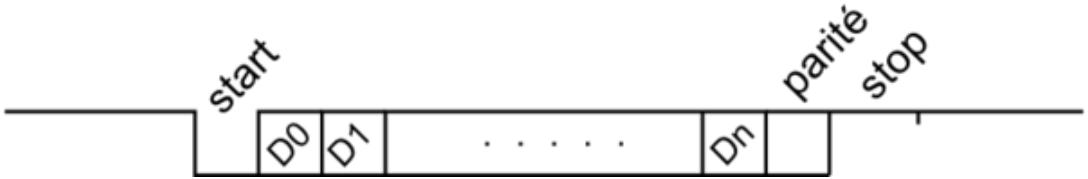

SPI Master
SCLK
MOSI
MISO
SS1
SS2
SS3
SCLK
MOSI
MISO
SS
SPI Slave
SCLK
MOSI
MISO
SS
SPI Slave
SCLK
MOSI
MISO
SS
SPI Slave

I2C



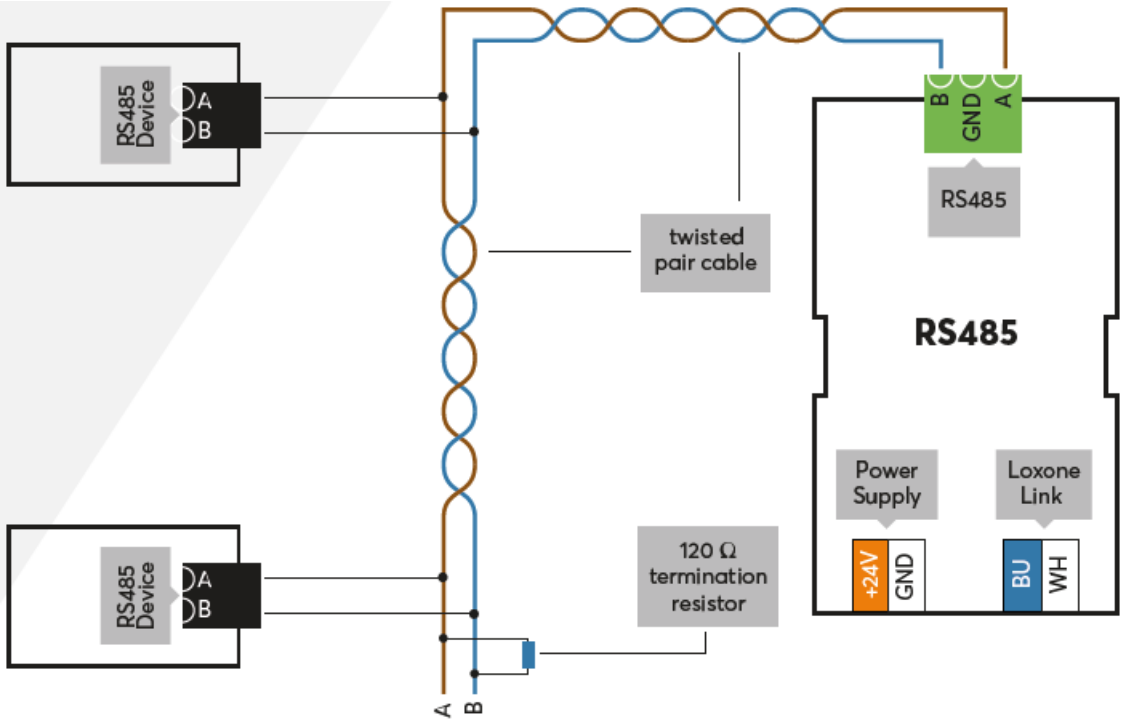
- Bus maître/esclaves
- 3 fils SDA, SCL et la masse
- Utilisation de résistances de tirage
- Emission de l'adresse à lire ou écrire puis la suite des données
- Peu de robustesse pour un routage inter-carte

UART



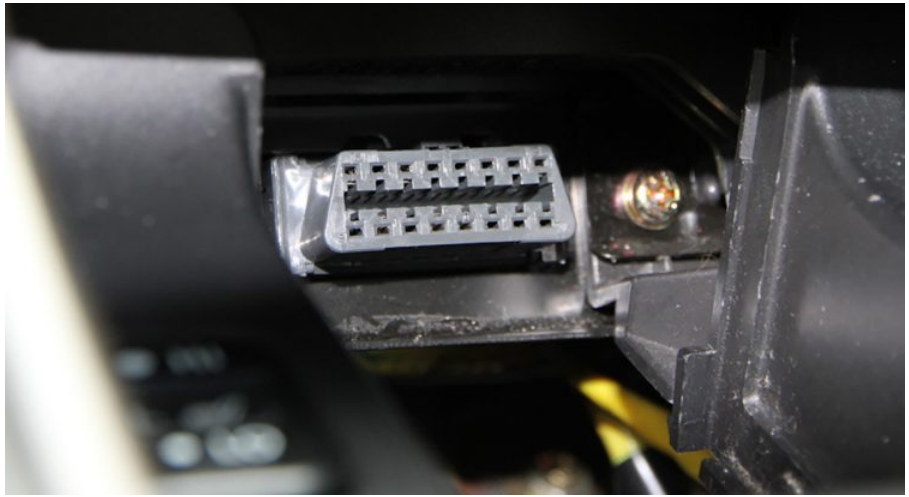
- Connexion full duplex (RX et TX)
- Bit de parité pour la détection d'erreur
- Très utilisé dans de nombreux systèmes (imprimantes, modems etc ...)
- Débit en bauds par seconde (1200, 2400, 4800, 9600, 115200 ...)
- Liaison point à point entre deux équipements

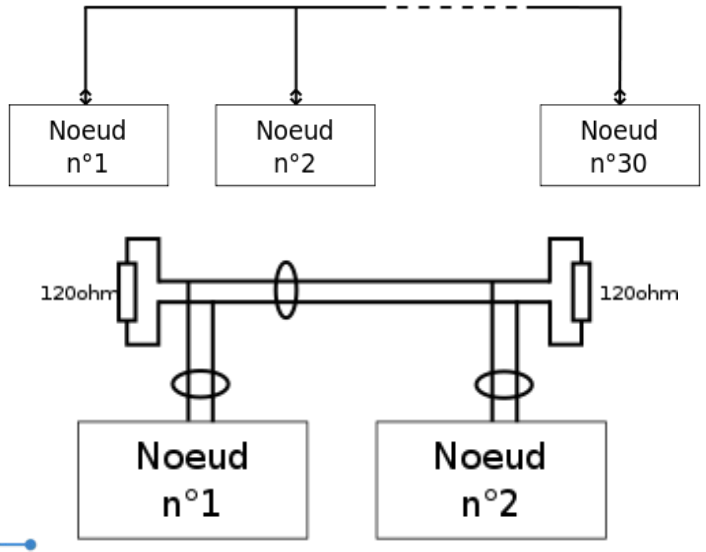
Bus RS385

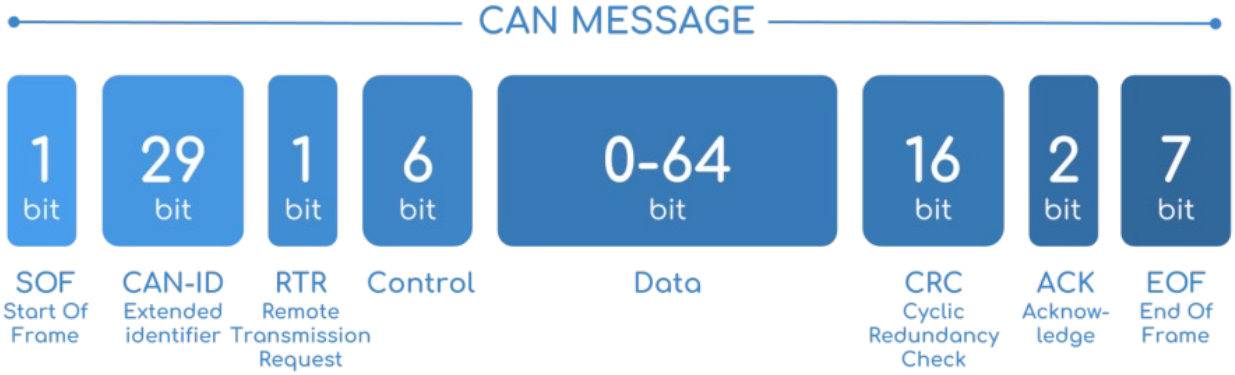


- Connexion multipoints
- Robuste aux interférences
- Utilisation de résistances de terminaison
- Souvent en mode maître/esclave
- Très utilisé dans l'industrie (Modbus)

Bus CAN







can-utils

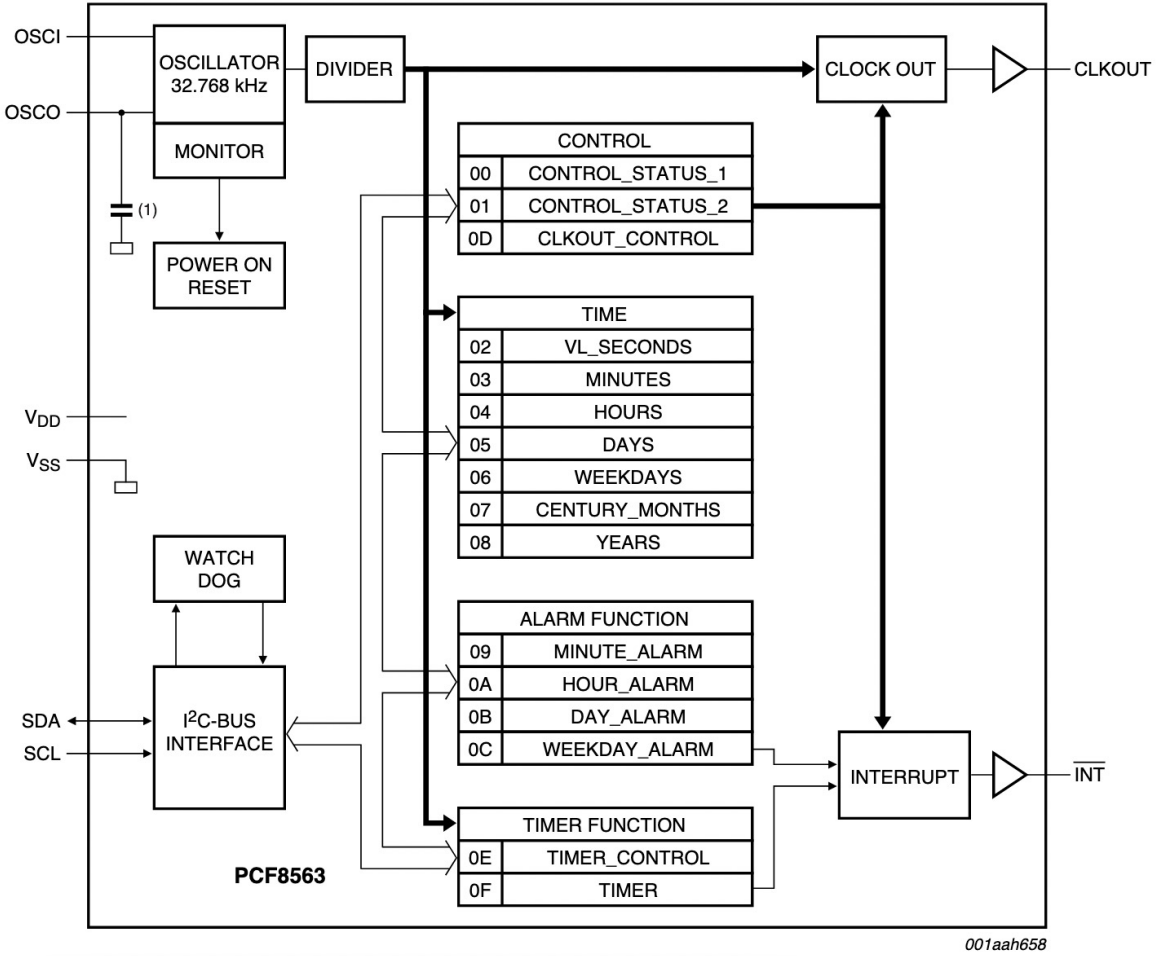
Périphériques

Puces électroniques auxiliaires

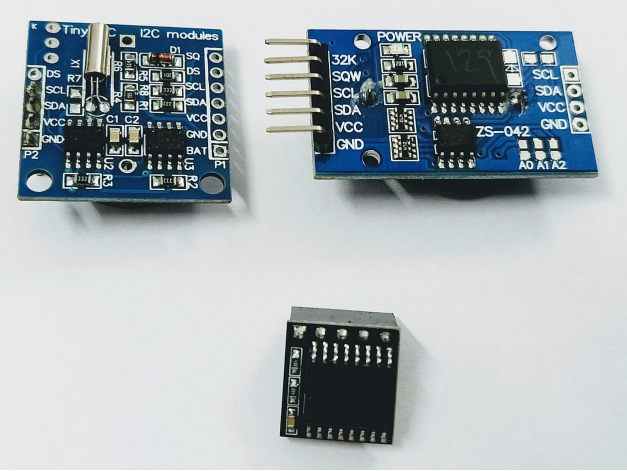
Horloge temps-réel

The frequency of a real time clock varies with the application. The frequency 32768 Hz (32.768 KHz) is commonly used, because it is a power of 2 (2^{15}) value. And, you can get a precise 1 second period (1 Hz frequency) by using a 15 stage binary counter.

Practically, in majority of the applications, particularly digital, the current consumption has to be as low as possible to preserve battery life. So, this frequency is selected as a best compromise between low frequency and convenient manufacture with market availability and real estate in term of physical dimensions while designing board, where low frequency generally means the quartz is physically bigger.



Horloge temps-réel



8.2 Register organization

Table 4. Formatted registers overview

Bit positions labelled as x are not relevant. Bit positions labelled with N should always be written with logic 0; if read they could be either logic 0 or logic 1. After reset, all registers are set according to Table 27.

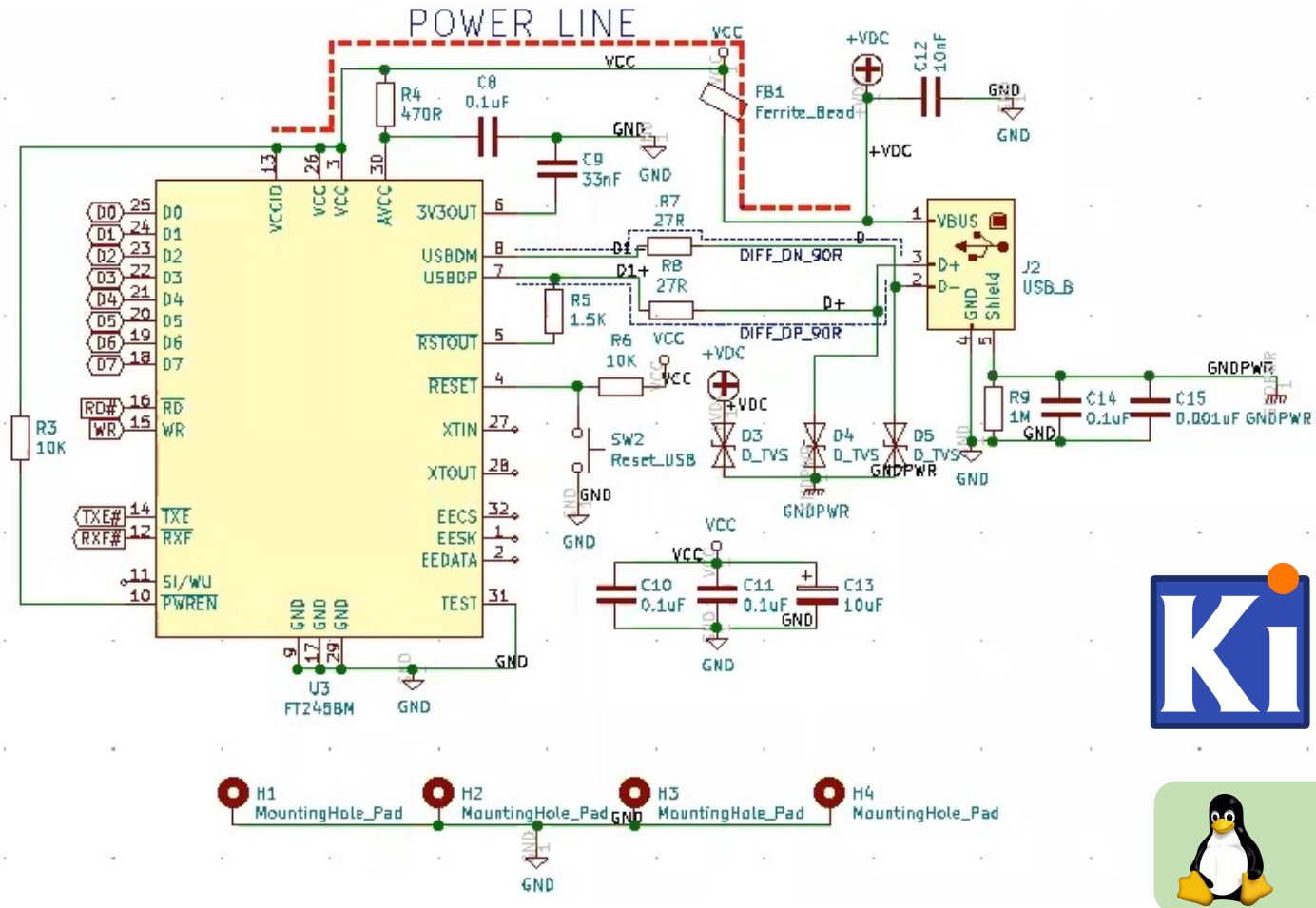
Address	Register name	Bit							
		7	6	5	4	3	2	1	0
Control and status registers									
00h	Control_status_1	TEST1	N	STOP	N	TESTC	N	N	N
01h	Control_status_2	N	N	N	TI_TP	AF	TF	AIE	TIE
Time and date registers									
02h	VL_seconds	VL	SECONDS (0 to 59)						
03h	Minutes	x	MINUTES (0 to 59)						
04h	Hours	x	x	HOURS (0 to 23)					
05h	Days	x	x	DAYS (1 to 31)					
06h	Weekdays	x	x	x	x	x	WEEKDAYS (0 to 6)		
07h	Century_months	C	x	x	MONTHS (1 to 12)				
08h	Years	YEARS (0 to 99)							

Address	Register name	Bit							
		7	6	5	4	3	2	1	0
Alarm registers									
09h	Minute_alarm	AE_M	MINUTE_ALARM (0 to 59)						
0Ah	Hour_alarm	AE_H	x	HOUR_ALARM (0 to 23)					
0Bh	Day_alarm	AE_D	x	DAY_ALARM (1 to 31)					
0Ch	Weekday_alarm	AE_W	x	x	x	x	WEEKDAY_ALARM (0 to 6)		
CLKOUT control register									
0Dh	CLKOUT_control	FE	x	x	x	x	x	FD[1:0]	
Timer registers									
0Eh	Timer_control	TE	x	x	x	x	x	TD[1:0]	
0Fh	Timer	TIMER[7:0]							

Conception des PCB

Schématisation, routage et impression

Schématisation des composants



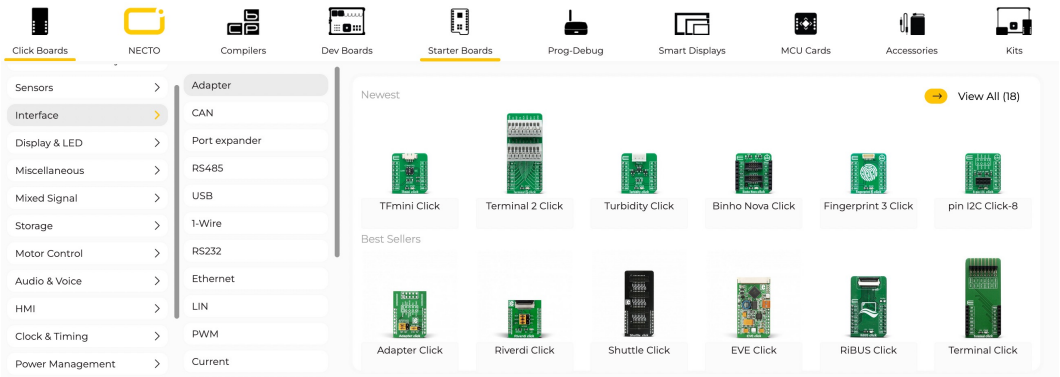
ALTIUM DESIGNER

KiCad

kicad

Comment trouver des circuits ?

https://www.mikroe.com/



https://www.ti.com/reference-designs

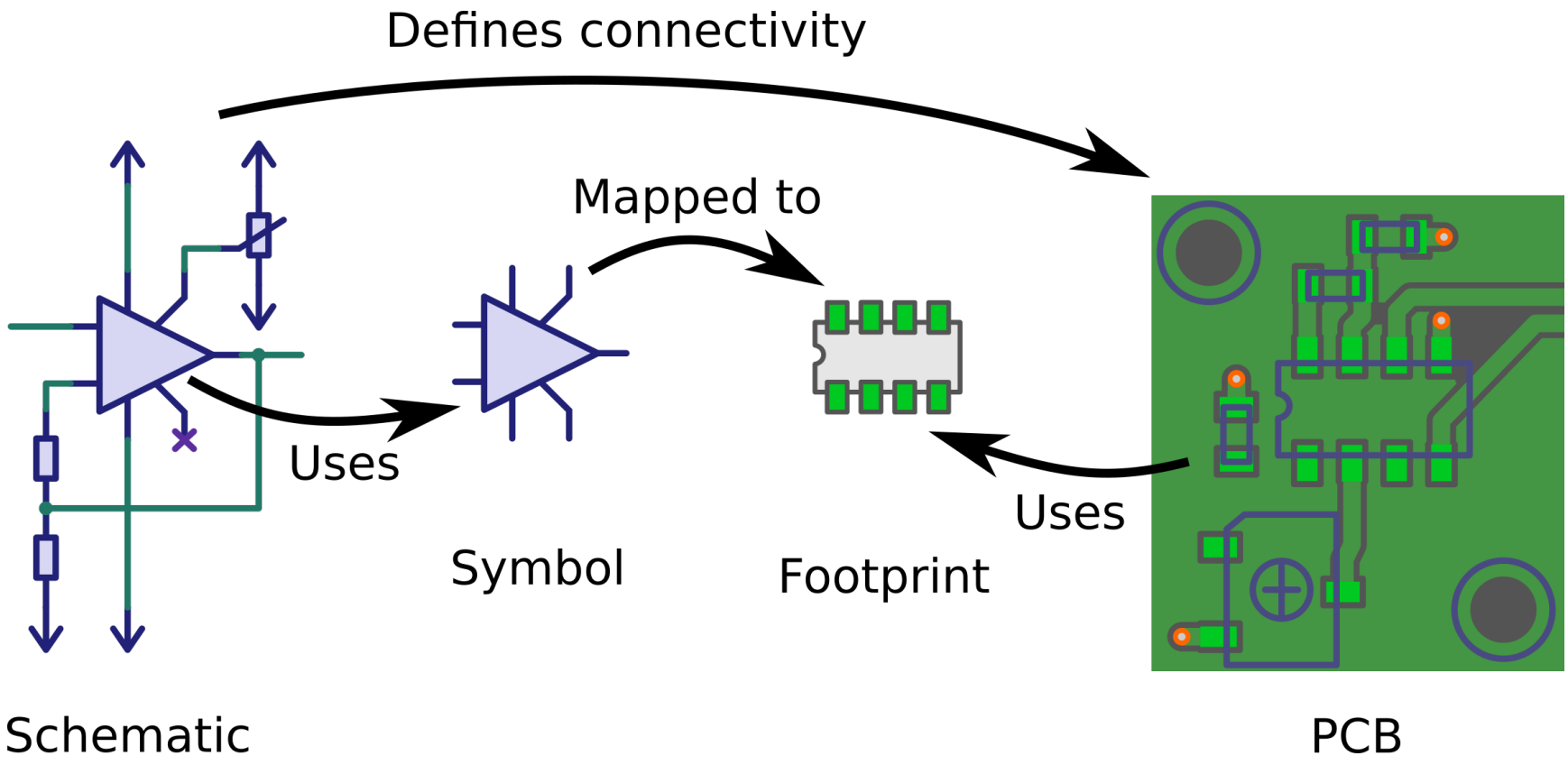
TIDA-00170

The TIDA-00170 is a reference design for industrial control Analog Mixed Input Output Modules. The design implements four channel analog input & two channel analog output. The analog input channels can measure all standard industrial voltages up to ±10V and current inputs up to 24mA. The (...)

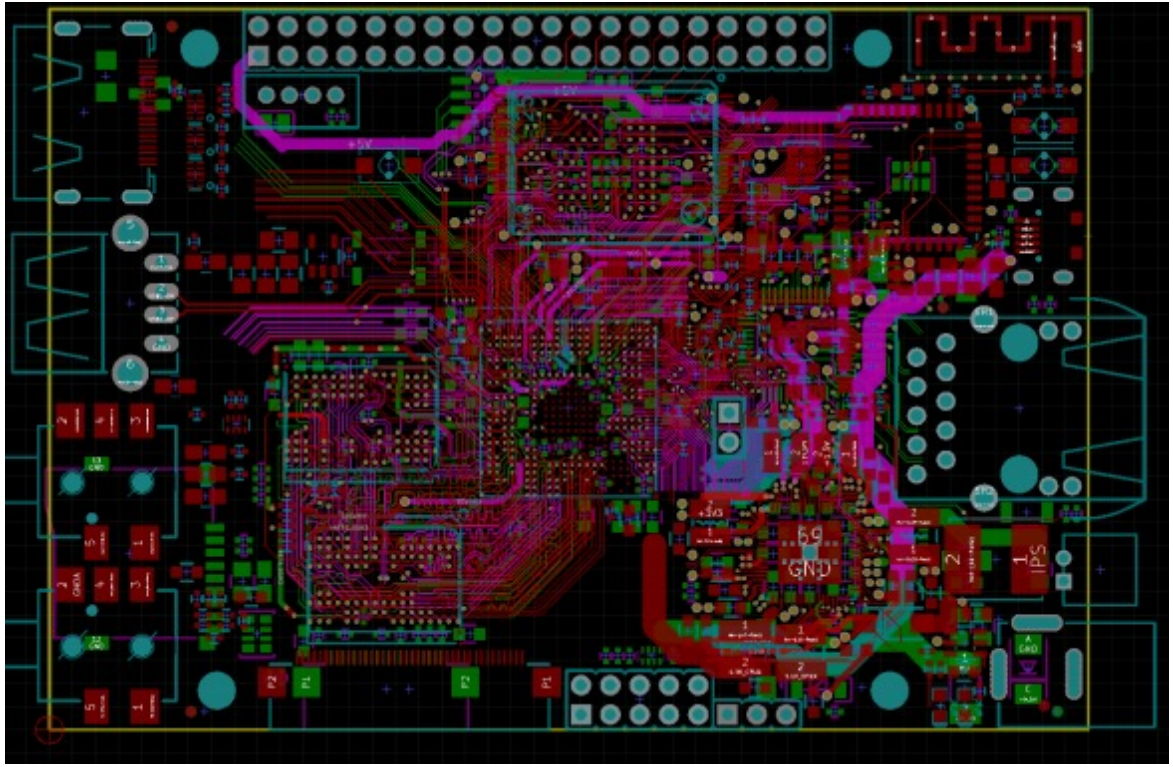
View design

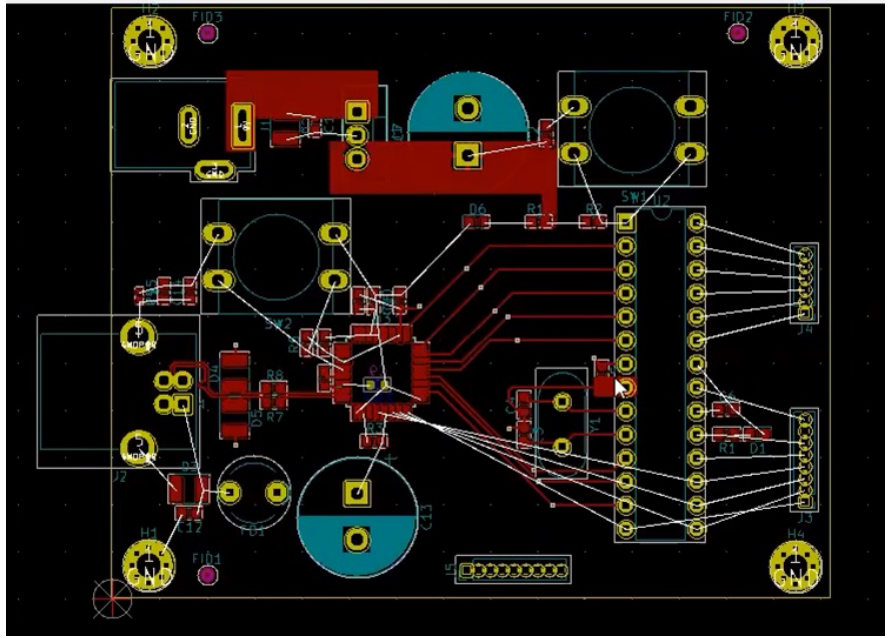
- Schematic
- CAD/CAE symbol
- Bill of materials (BOM)
- Assembly drawing
- PCB layout
- User's Guide
- Description & features
- Technical documents
- TI devices
- Support & training

Association des schémas avec les empreintes



Routage des cartes électroniques

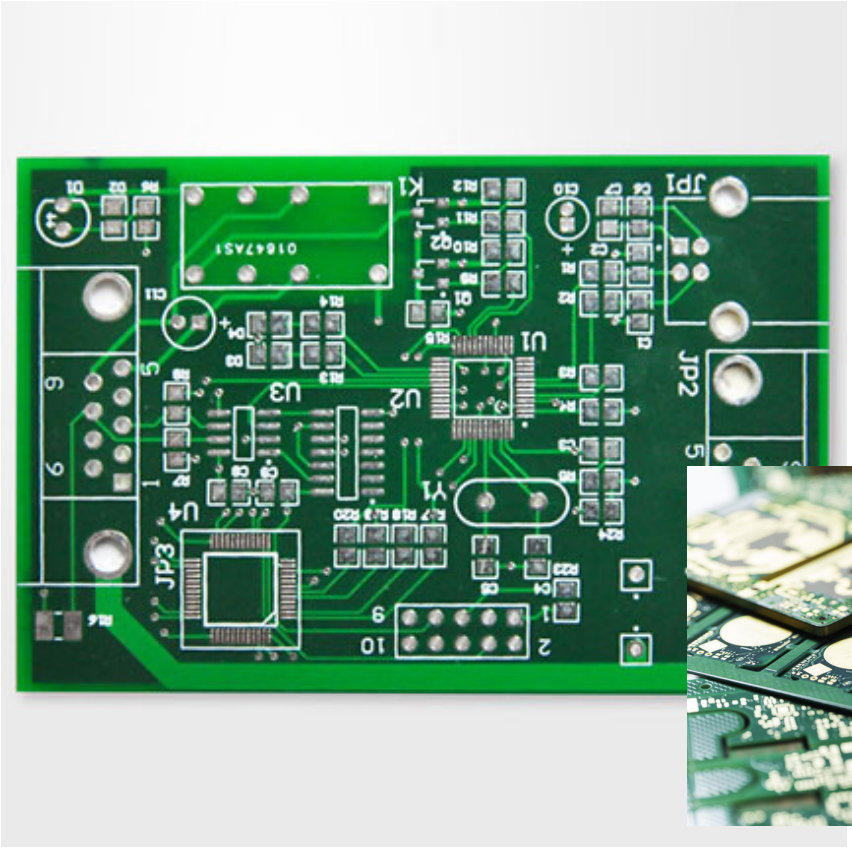


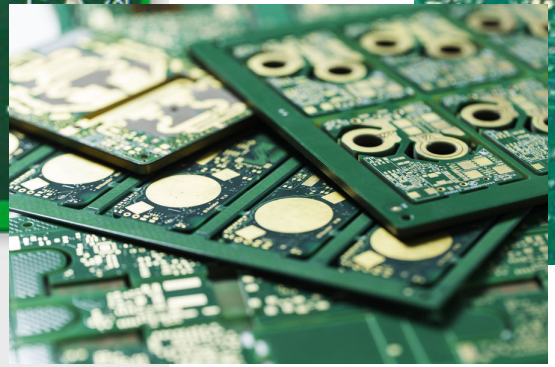


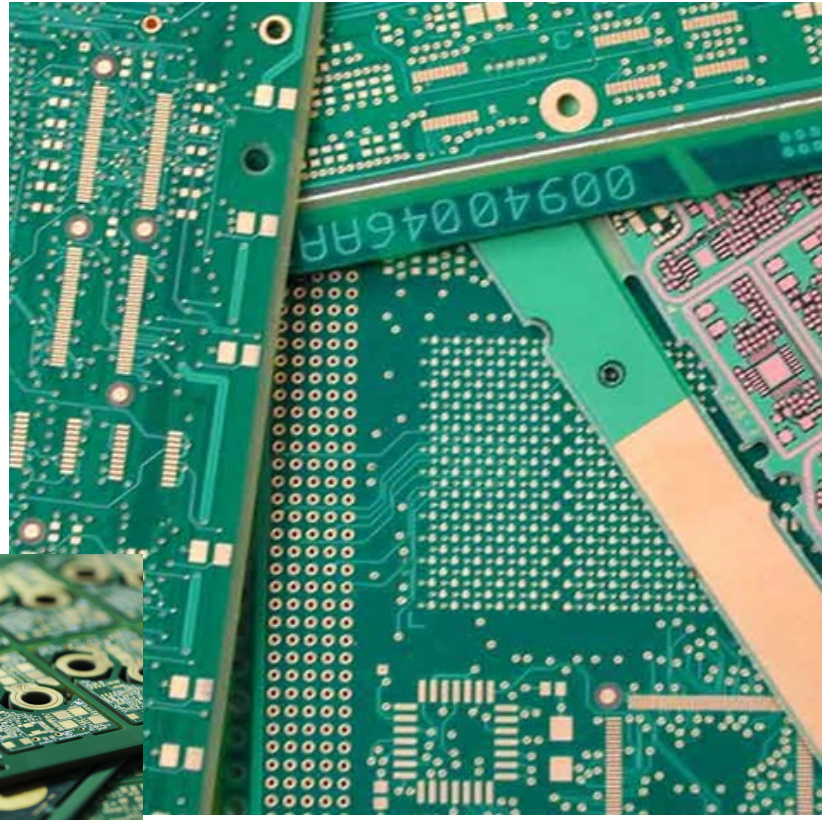
Tirage des cartes électroniques

Aisler

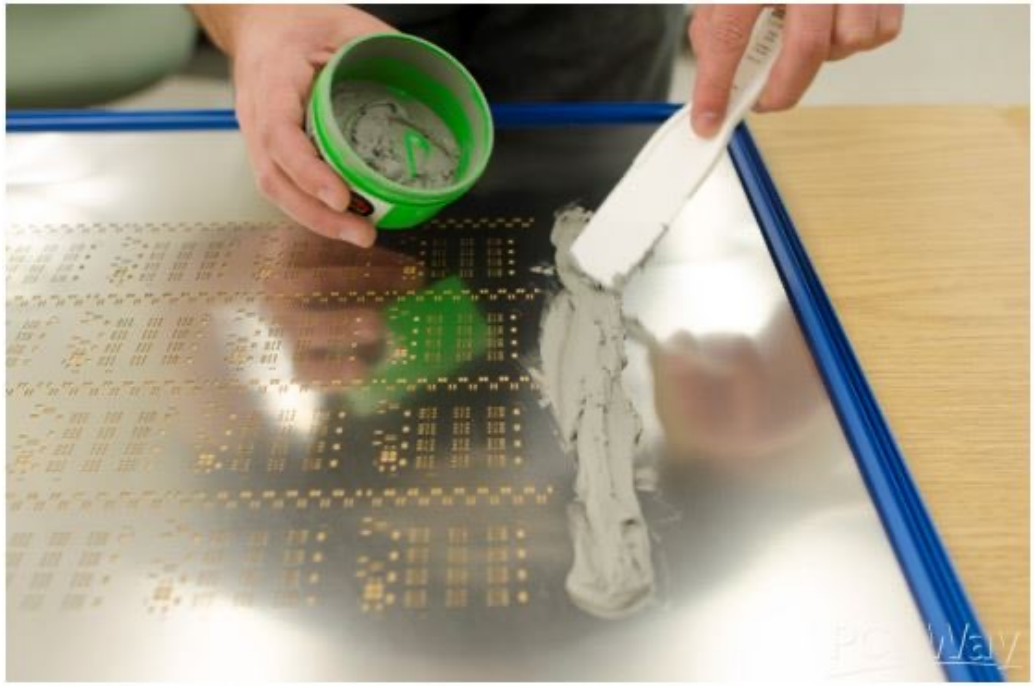
Tirage des cartes électroniques

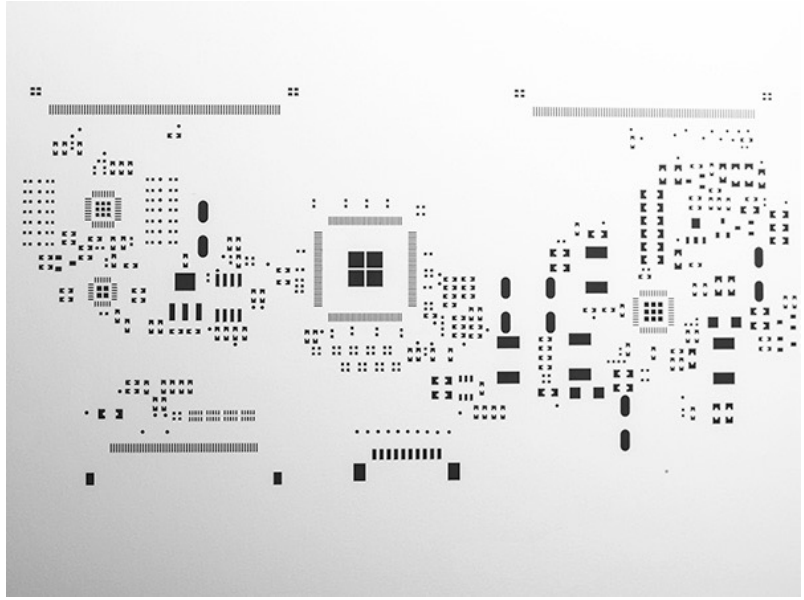




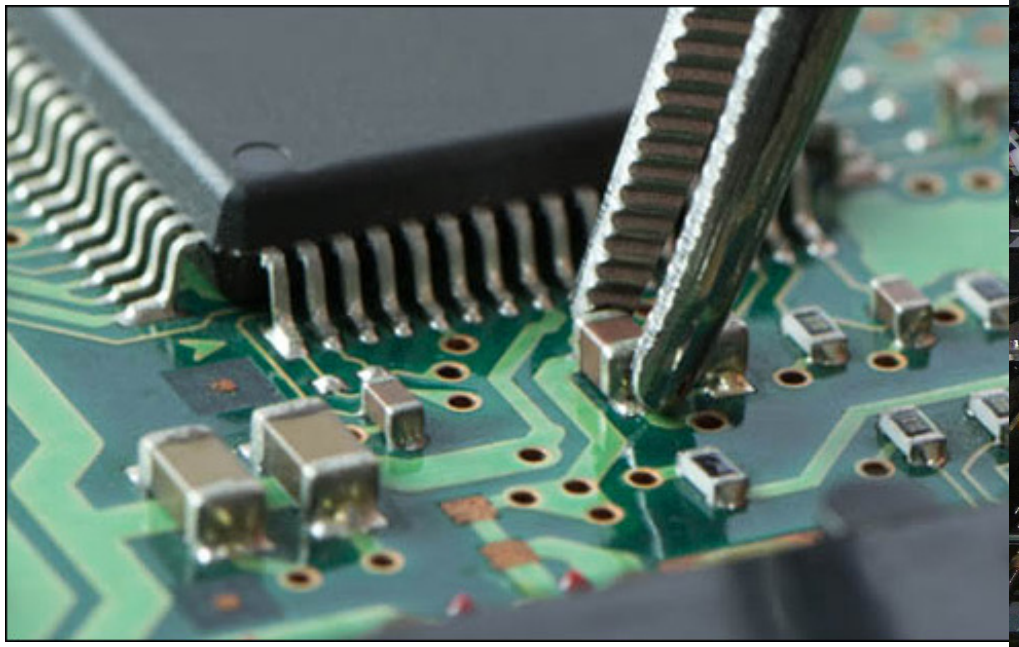


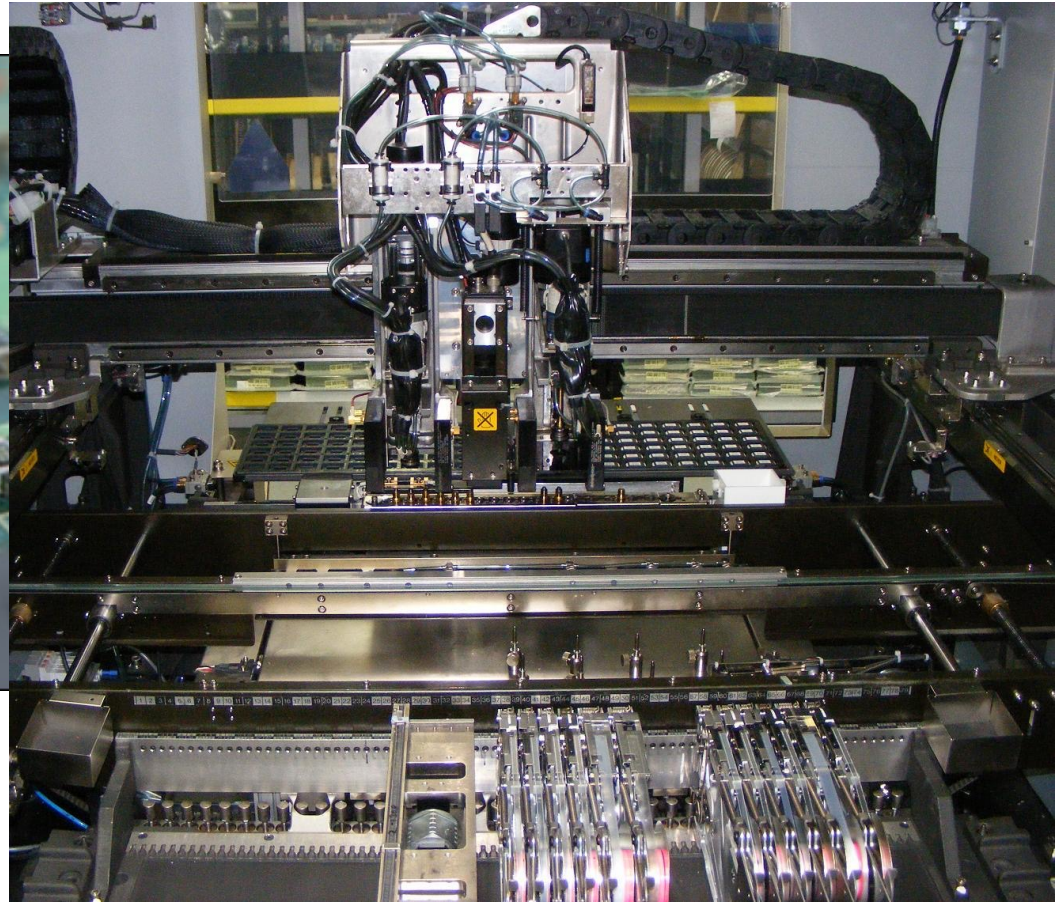
Usage d'un stencil pour la soudure des CMS



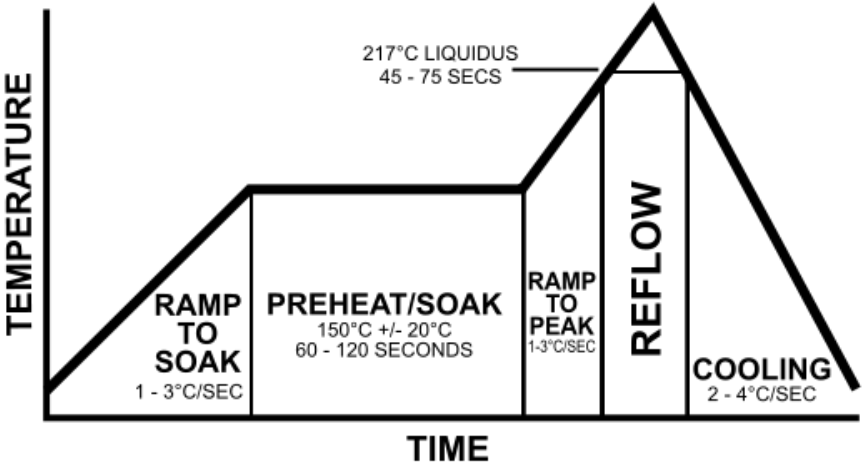


Placement des composants





Soudure au four à refusion

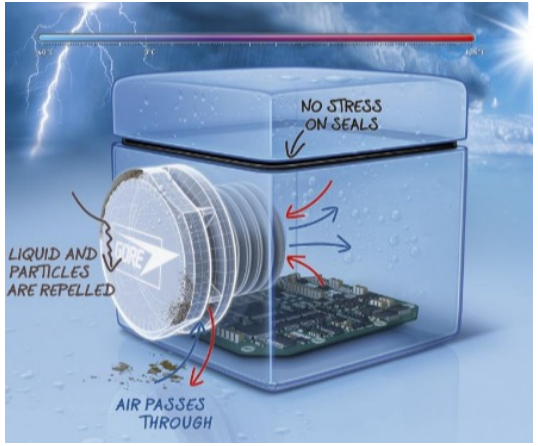


Adaptation à l’environnement

Conditions hostiles des systèmes embarqués

Eau et humidité

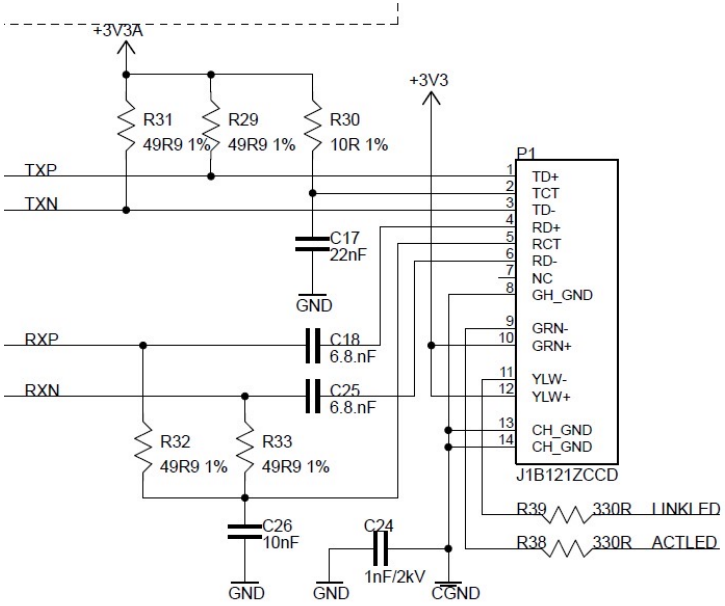
GORE® Protective Vents are available in many different sizes and designs and can be easily integrated into new or existing design structures. The screw-in PolyVent M12 x 1.5 HA reliably protects the FL42 halogen lamp made by WE-EF from the most adverse weather conditions and temperature differences.

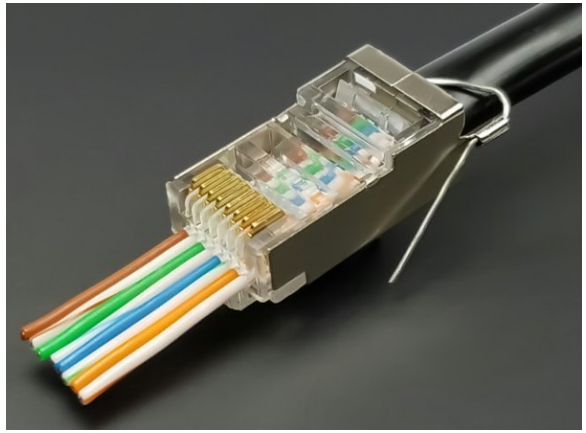


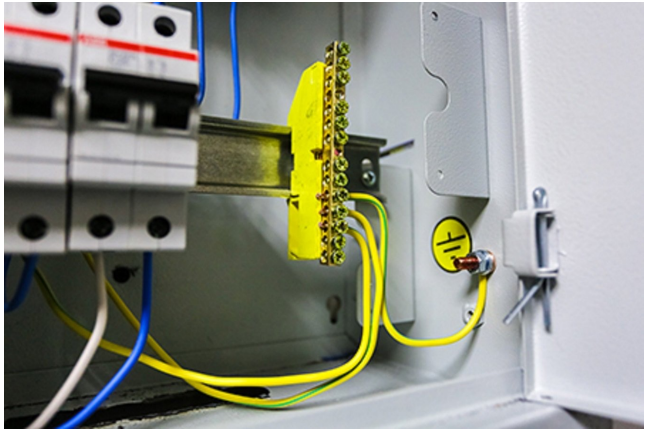
Tropicalisation des cartes électroniques

- Humidité / condensation
- Eau salée
- Vibrations
- Températures élevées
- Cycles thermiques
- Courts-circuits à cause de saletés

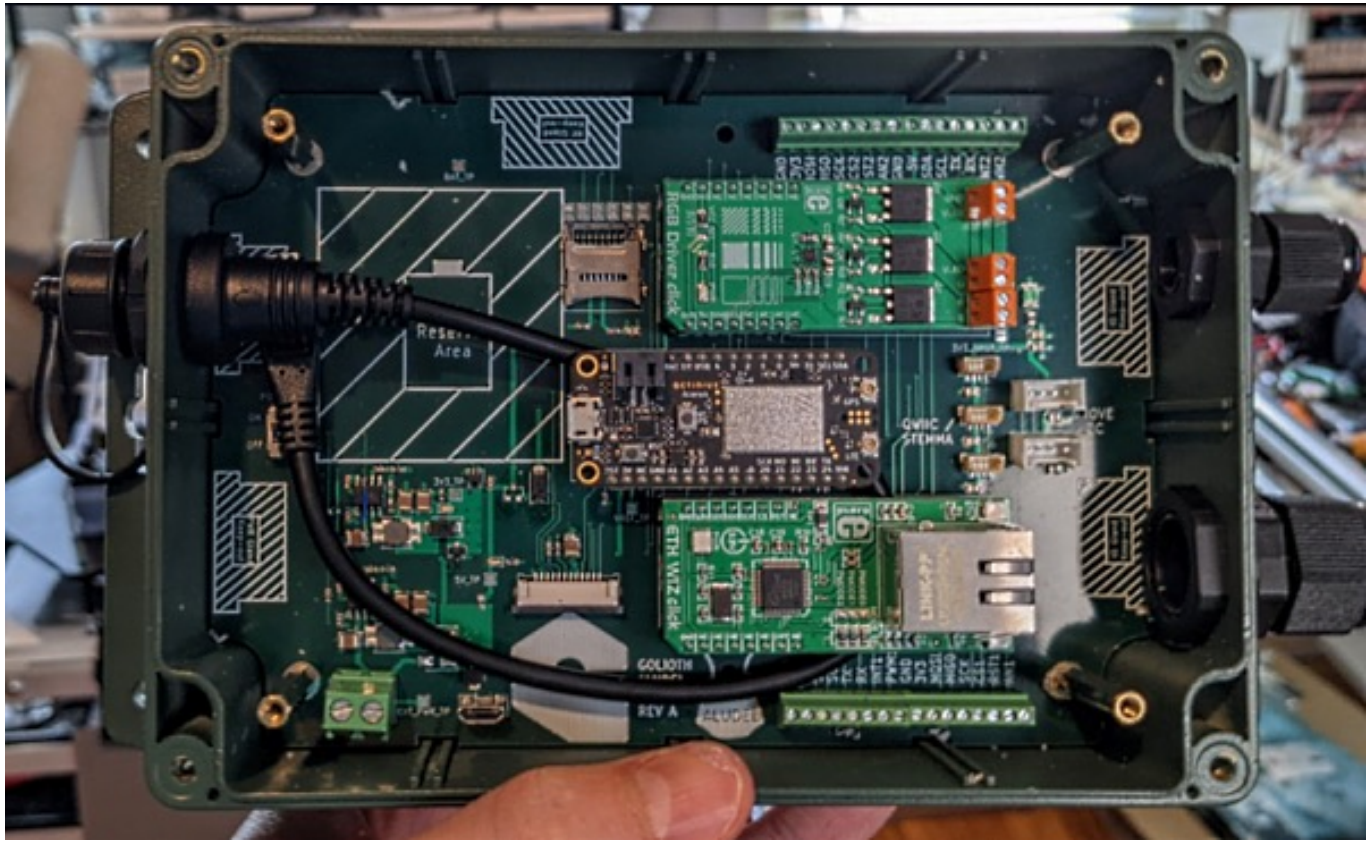
Compatibilité électromagnétique

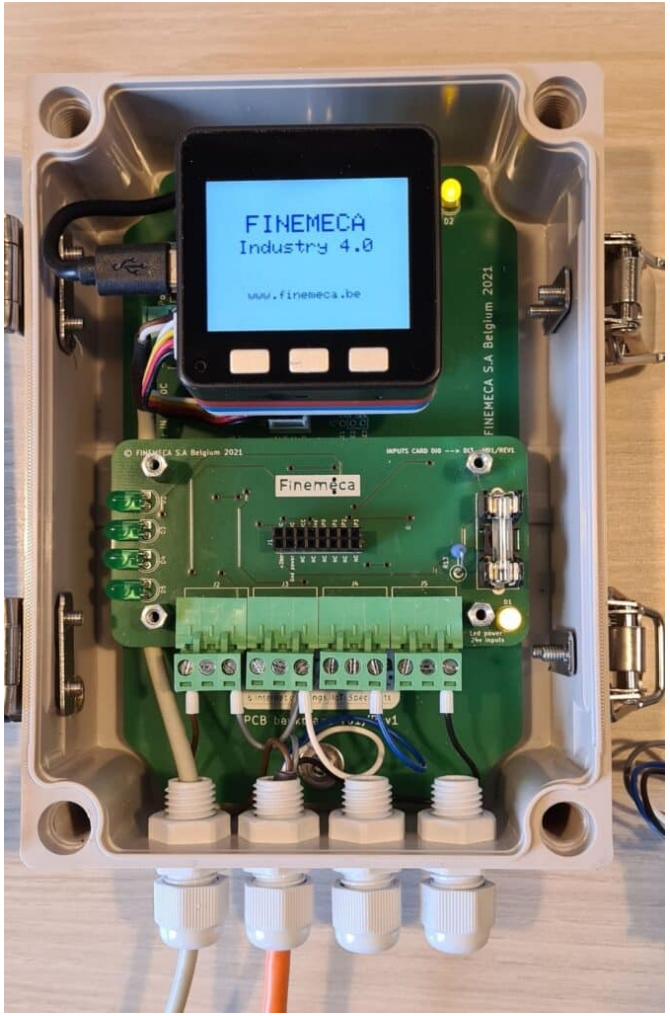




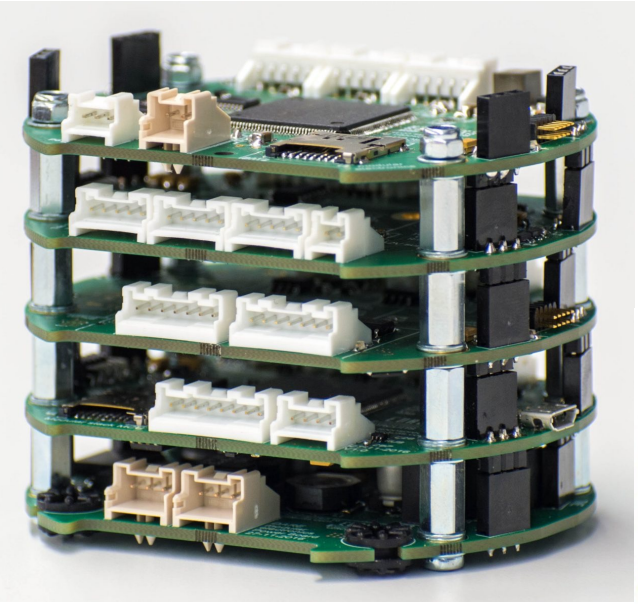


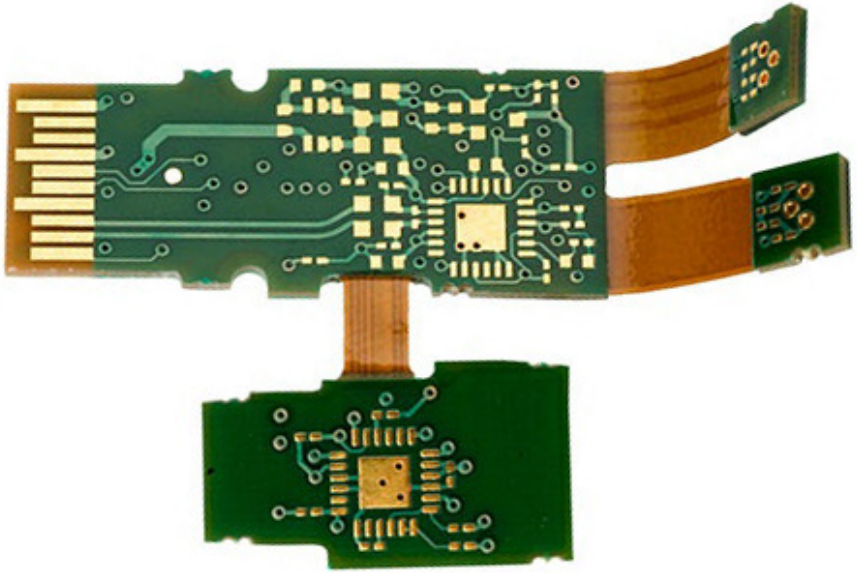
Résultat d'intégration de prototypes





Connexions entre plusieurs cartes



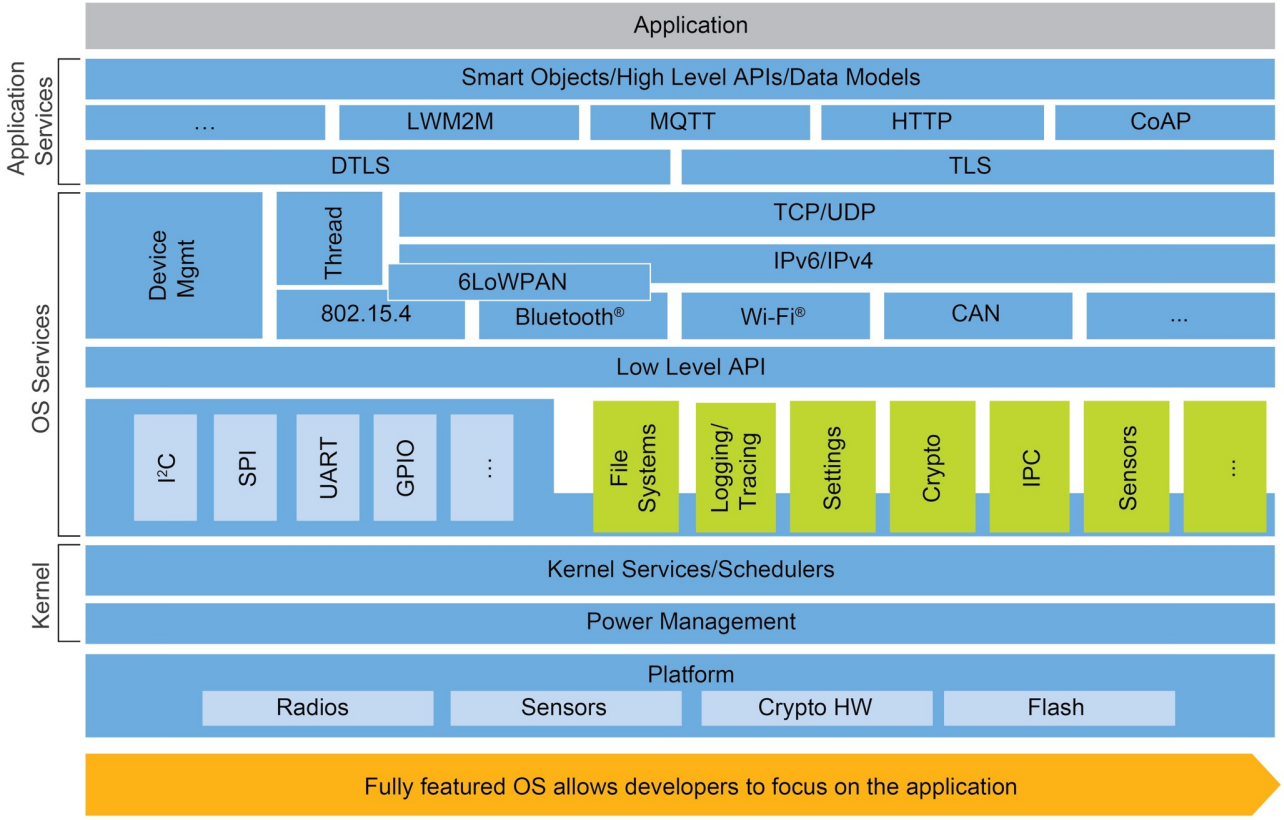


Logiciels embarqués

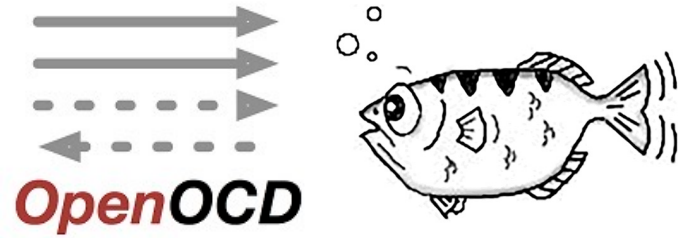
Framework et bibliothèques

Framework Arduino

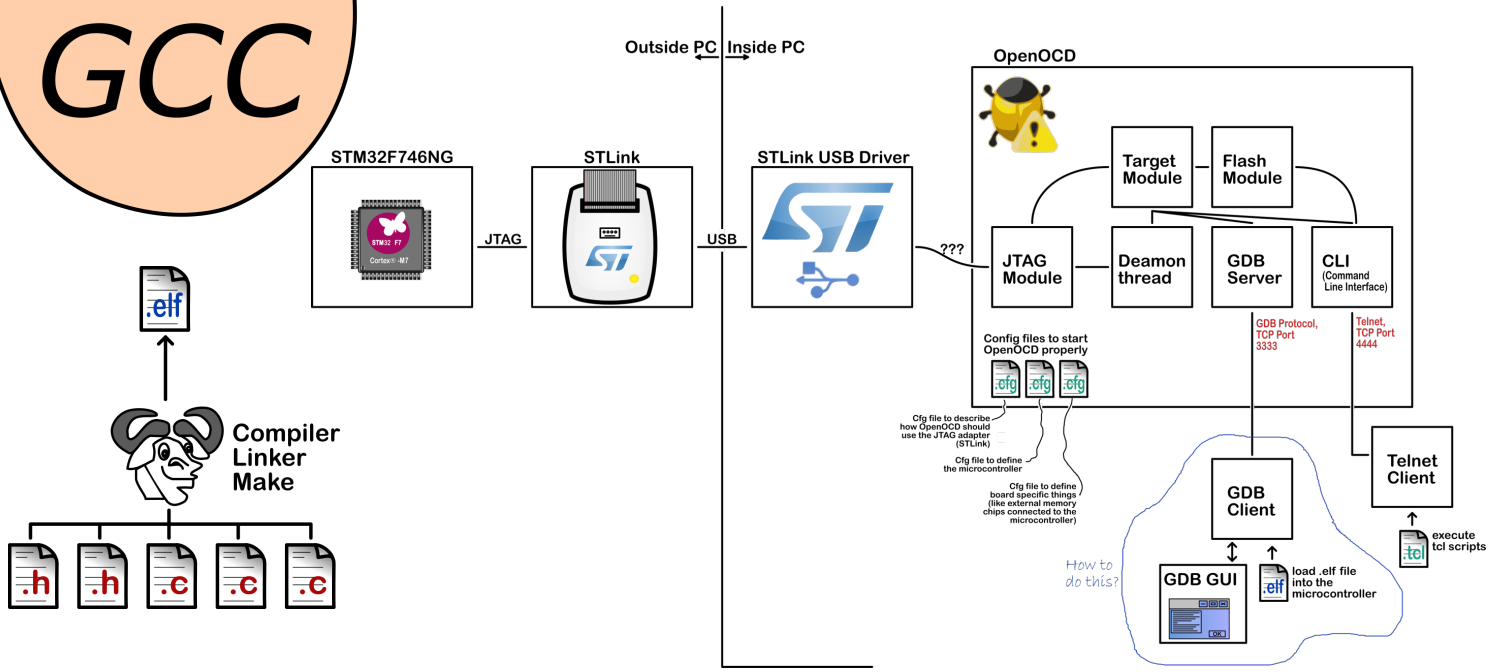
Framework Zephyr

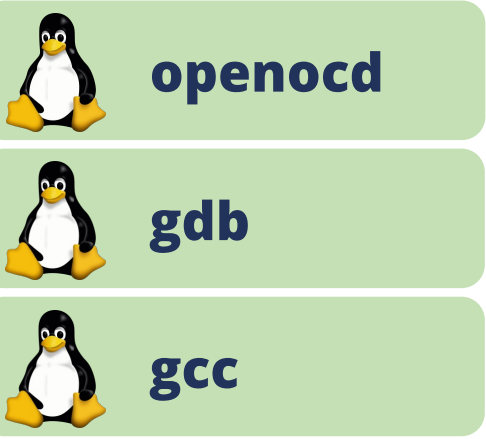


Compilation et flashage d'un microcontrôleur

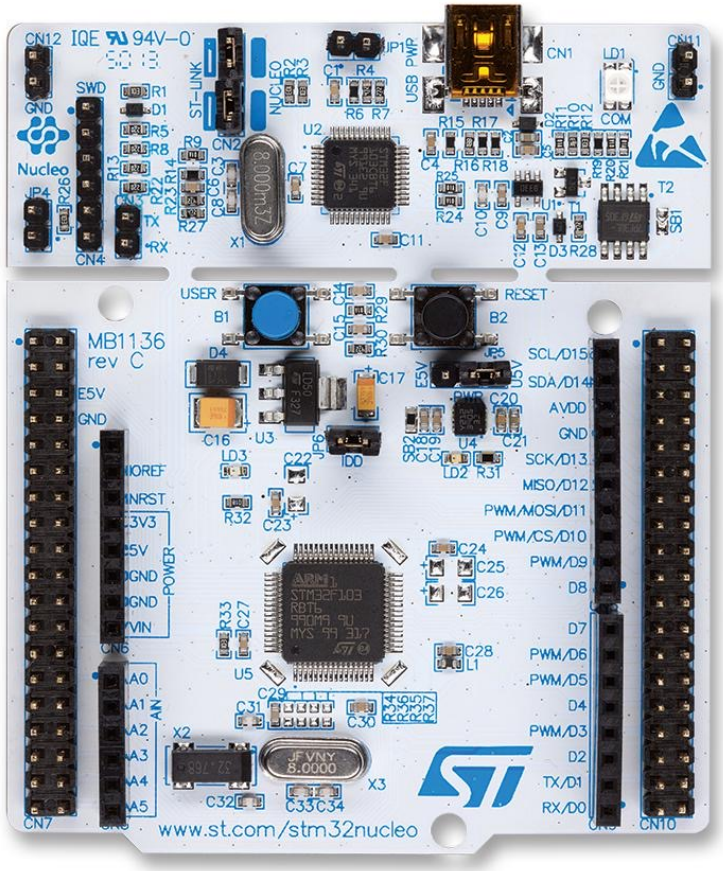


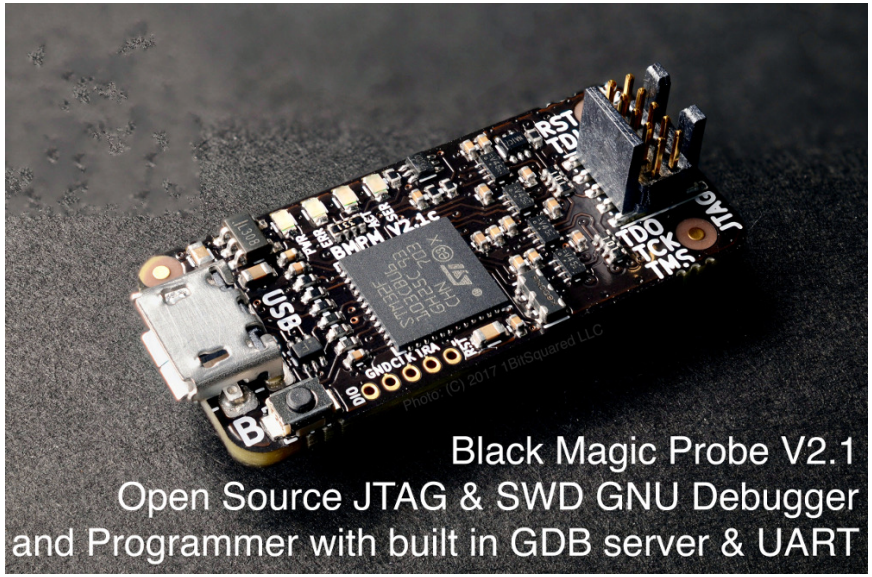
GDB
The GNU Project Debugger





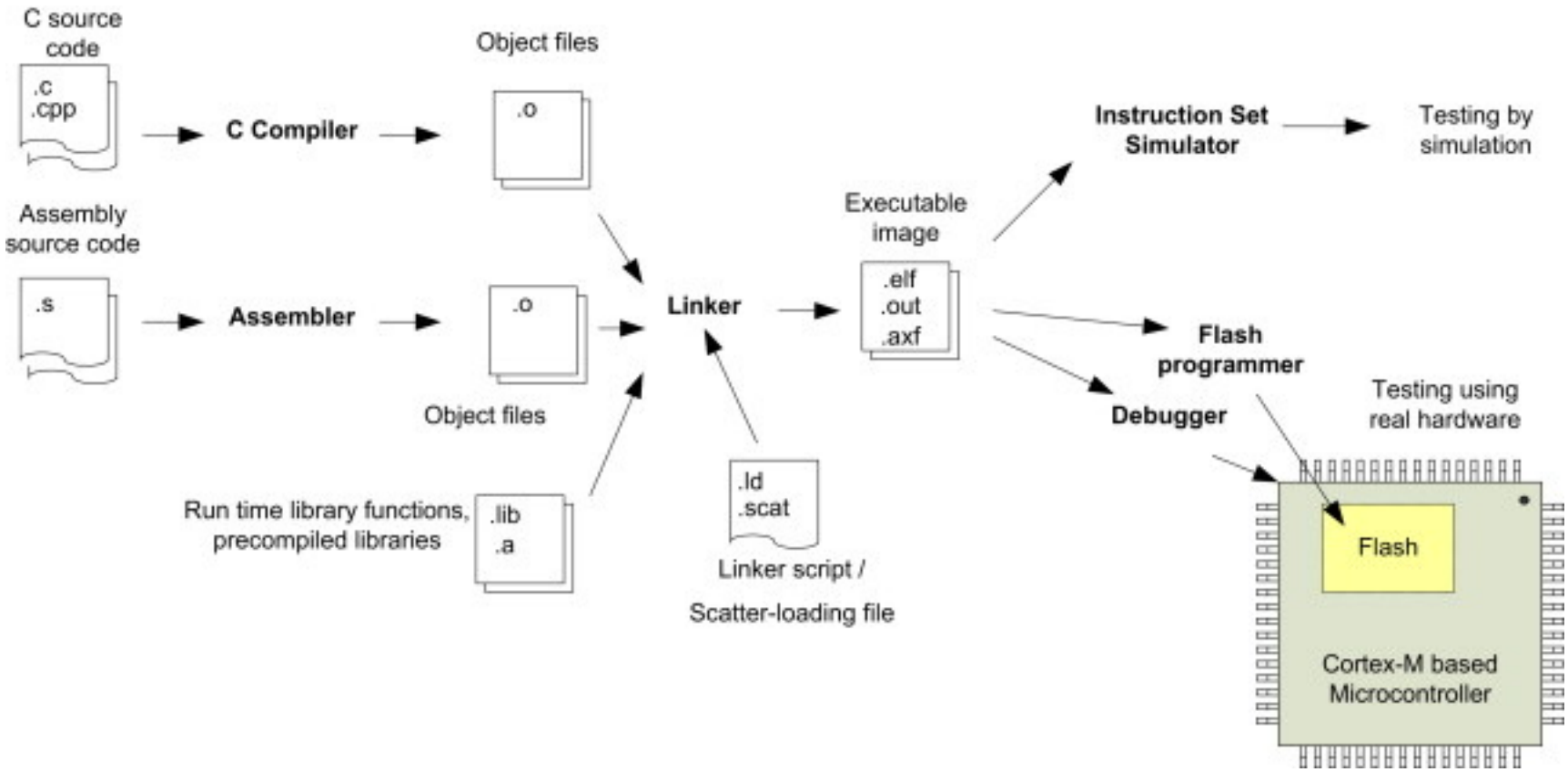
Sondes de debug et debugger in situ



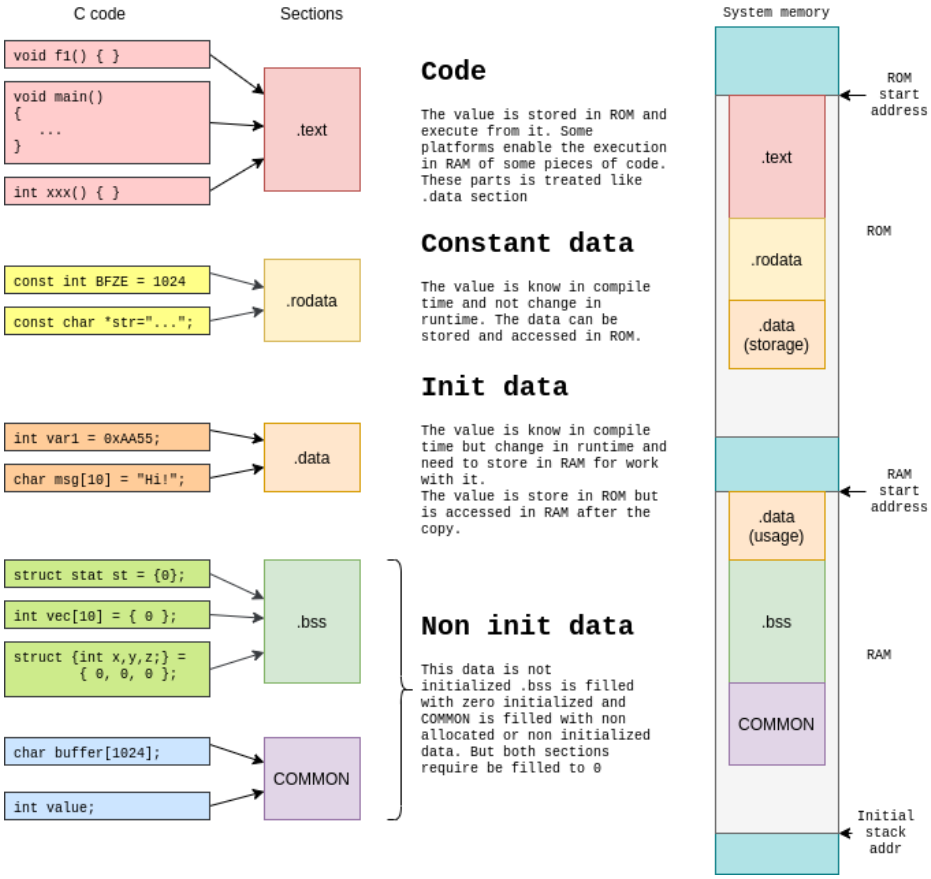


BMP

Compilation et flashage d'un microcontrôleur



Compilation et flashage d'un microcontrôleur




```
/* Start of section description layout */
SECTIONS
{
  . = 0x08000000; /* The dot is current address counter. */

  /* If you do not specify any, start at 0 */
  .text : {
    /* KEEP keyword is used to  ensure that symbols are not discarded if the
       linker is instructed to remove unused symbols. */
    KEEP(*(.vector_core*)) /* Place .vector_core at start of ROM */
    *(.text)   /* Place all symbols in ".text" section */
    *(.text.*)  /* Place all symbols that start with section ".text.<any>" */
  }

  /* In many platforms, the linker script puts the .rodata in .text if
     the corresponding section does not exist */
  .rodata : {
    . = ALIGN(4); /* Ensure word alignment of sections */
    *(.rodata)
    *(.rodata*)
    . = ALIGN(4); /* Ensure word alignment of sections */
  }

  .init_array : {
    . = ALIGN(4); /* Ensure word alignment of sections */
    __init_array_start = .;
    /* SORT function sorts the symbols listed in alphabetical order.
       This is required to meet with the initialization order.
       All symbols are in the form of .init_array.0000_nameofsymbol
       when 0000 is replaced by a priority number that can be specified
       at compile time. */
    KEEP(*(SORT(.init_array.*)))
    KEEP(*(.init_array))
```