Heterogeneous Embedded Multicore Design Graduate Education in ENSTA PARIS: A 5 years Feedback

Omar Hammami
ENSTA PARIS
828 Bvd des Maréchaux
91762 Palaiseau
France
hammami@ensta.fr

Outline

- Introduction
- Embedded multicore
- Training and education
- Training architecture Sept – January Span (42 H)
- HLS course and project
- Embedded Multicore course and project
- Students projects
- Conclusion and perspectives

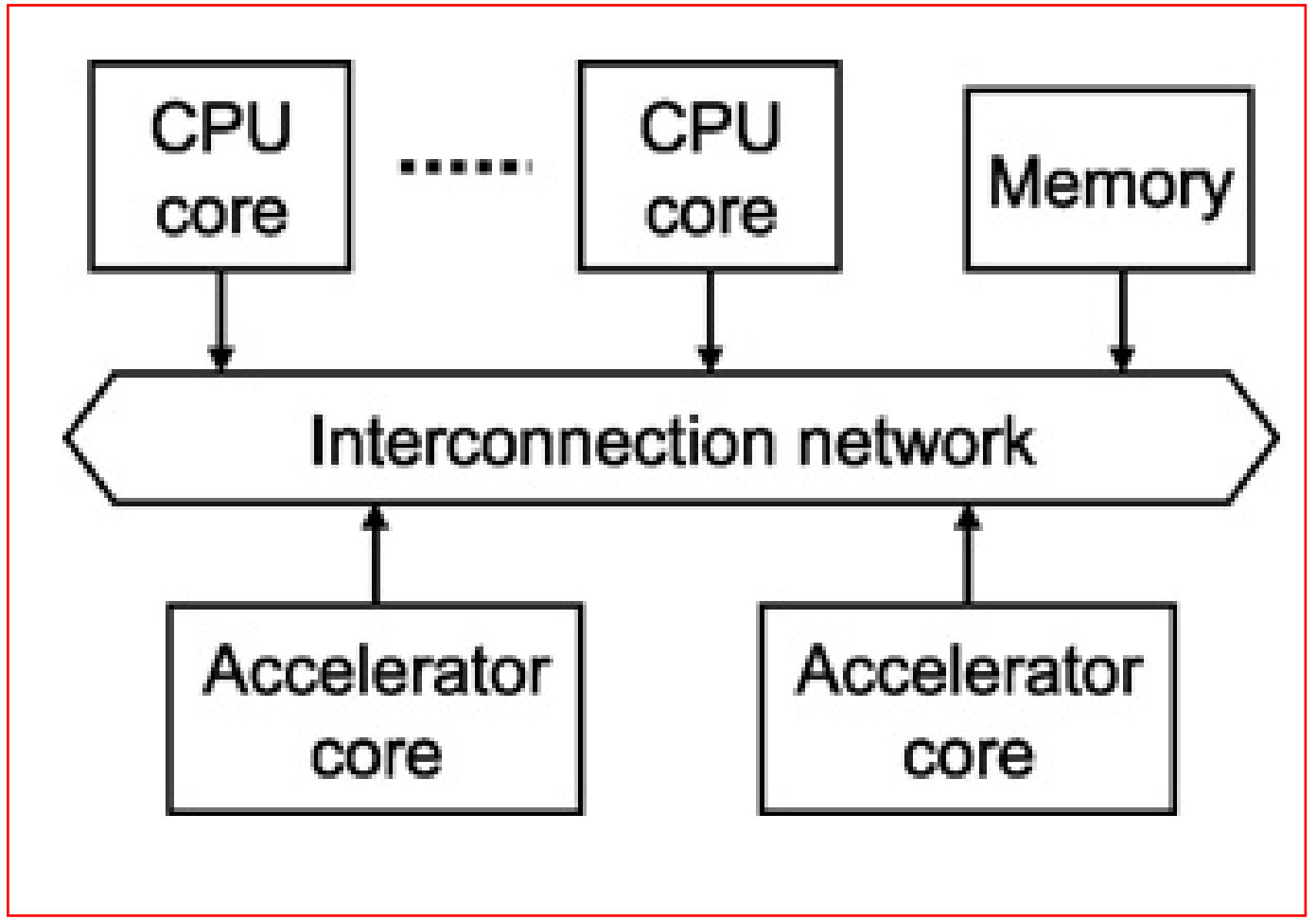
Introduction - Motivation

- Embedded systems are widespread and in strong growth in multiple industries (defense/aerospace/communications/transport/…)
- Complexity of embedded systems is increasing with Moore's Law exponential growth
- Embedded systems a strategic technology in defense companies with no outsourcing possibilities
- Systems complexity in industry requires sustained and matching increased engineering skills
- Semiconductors industry growth can't keep up without matching skills and associated design productivity

Heterogeneous Embedded Multicore

- Multicore have emerged strongly in embedded devices (cellphones, industrial equipments, etc°
- Homogeneous Multicore (a.k.a symmetric) present same embedded processor configuration
- Embedded systems offer the opportunity of full customization of embedded IPs: configurable soft IP processors, Network on Chip, hardware accelerators , embedded memories, to match performance, resources and cost constraints
- Heterogeneous embedded multicore mixes heterogeneous embedded processors IP and HW accelerators
- FPGA offers a natural testbed for Heterogeneous Embedded Multicore (a.k.a HMP – Heterogeneous Multi-core Processing)

Heterogeneous Embedded Multicore Architecture – Single Chip



- Fully customizable Ips
- Design Space Exploration
- NP-hard problem

Training and Education

- Graduate level education in ENSTA PARIS: ROB306 (HLS and Hardware accelerators) and ROB307 (Heterogeneous Embedded Multicore MPSOC)
- **Objectives on FPGA Platforms (Xilinx)** :
  1. design, implementation and optimization of complex embedded systems
  2. discover, understand and master potentials of FPGA Technology
  3. design of hardware accelerators under energy/area/performance constraints
  4. design of embedded multicore with emphasis on NOCs (Network on Chips)
  5. Parallel programming
  6. Automatic Design Space Exploration and MDAO
- Strong interaction with industry for embedded systems skills requirements (Qualcomm, Arteris, SiPearl,MBDA, …): internships/job opportunities/research programs

Training Architecture

2 graduate courses 2 x 21H – Sept - Dec

ROB 306

HLS – FPGA – HW-Sw Codesign
Zedboard – Vivado CAD tool
HLS project 1
Zedboard execution – IVVQ
Zynq Book and Tutorials
Reference

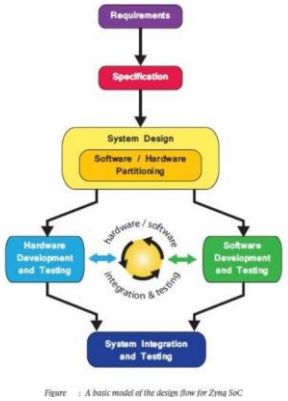
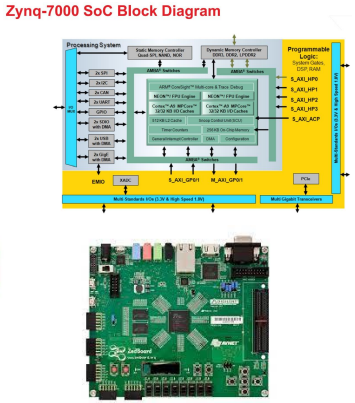
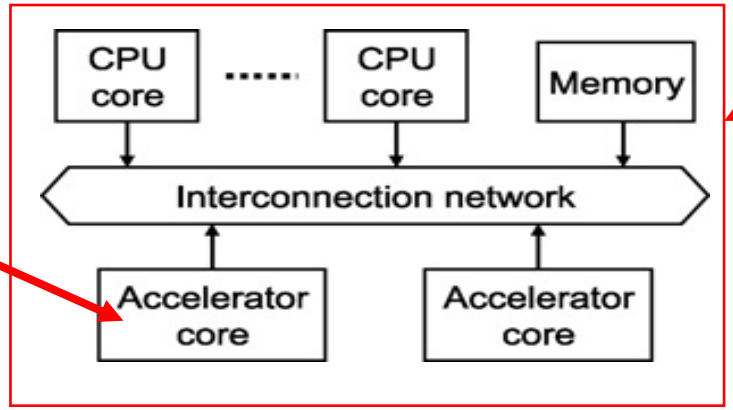


Figure : A basic model of the design flow for Zynq SoC

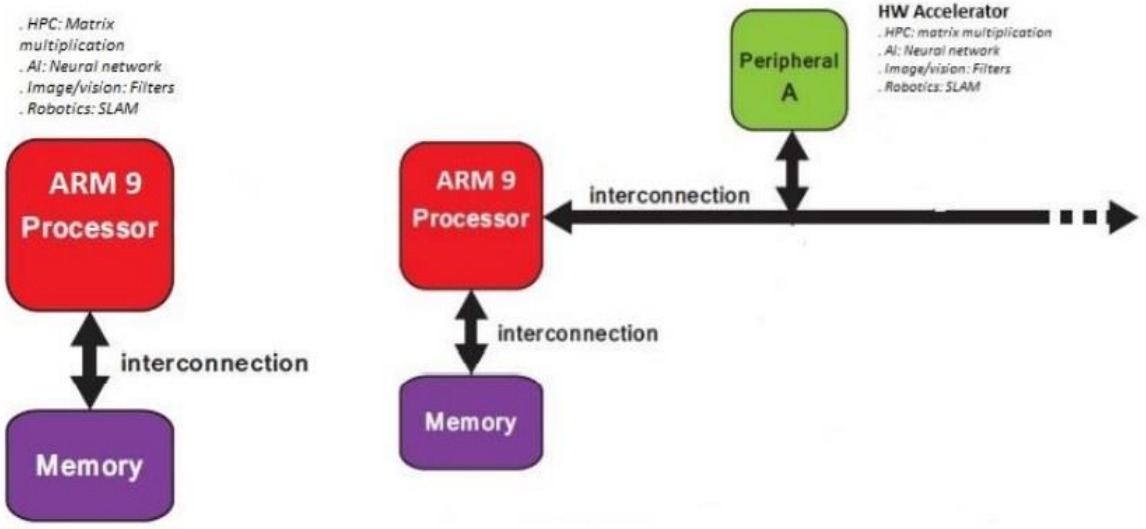


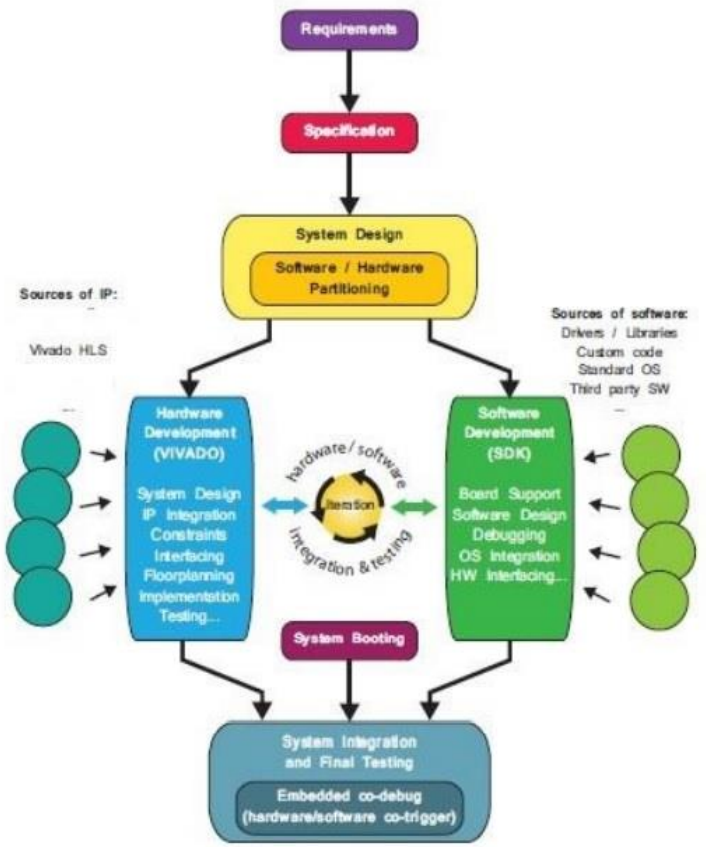


ROB 307

Network on Chip (AXI)
Heterogeneous Multicore
Project 2
5 processors multicore
ARM9 + 4 MB
+ HW accelerators
Zedboard execution IVVQ

Embedded Systems Hw-Sw Codesign



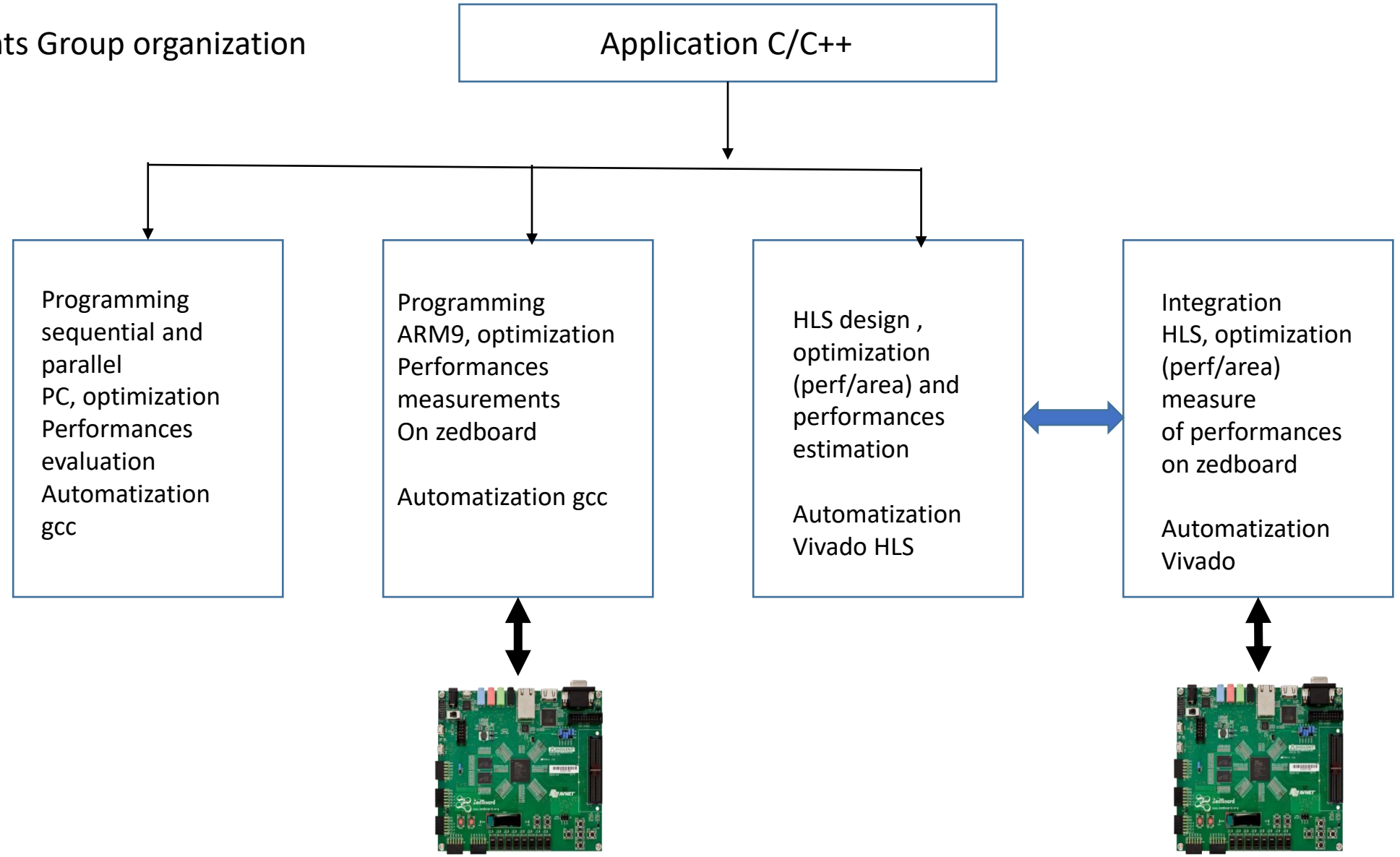


: The design flow for Zynq SoC (expanded model)

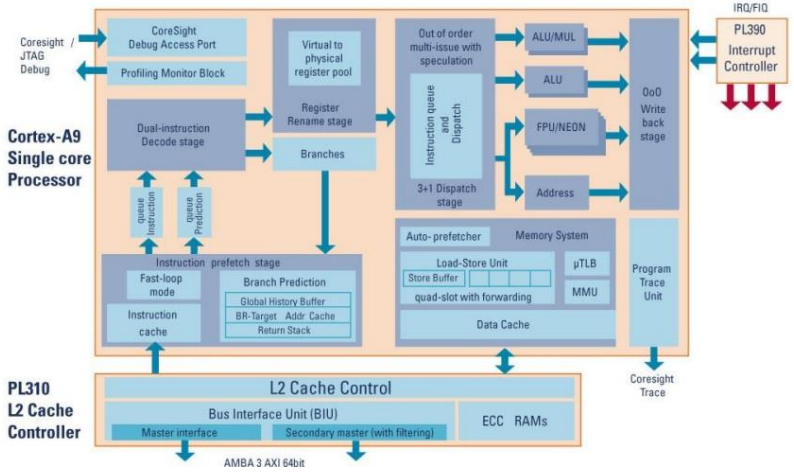
ROB 306 – Hw/Sw Codesign

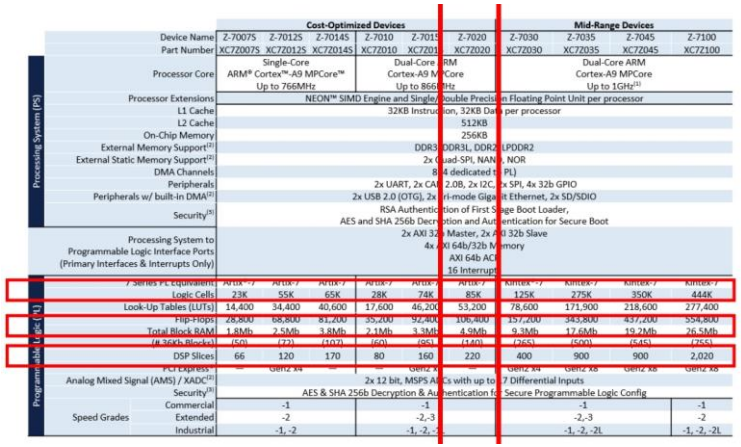
- **Q1.** PC software performance evaluation – algorithms variations, compiler options explorations, parallel programming (multi-threads, OpenMP, etc…)
- **Q2.** Embedded processor Performance evaluation ARM9 – C code Vivado 2019 SDK – explore all possible optimizations microarchitecture du processeur (caches, branch prediction superscalar execution units , dual-core)
- **Q3.** HLS Design, synthesis and synthesis options exploration – Performance/Area tradeoffs latency, bandwidths – resources XC7Z020 (logic cells (% de 85K), LUTs (% de 53200), Block RAM (% de 4,9 Mb), DSP slices (% de 220). TCL epxloration
- **Q4.** Hardware Implementation on zedboard and execution
- **Q5**. Automatic Design Space Exploration of Hw accelerator inside the embedded systems structure

Students Group organization



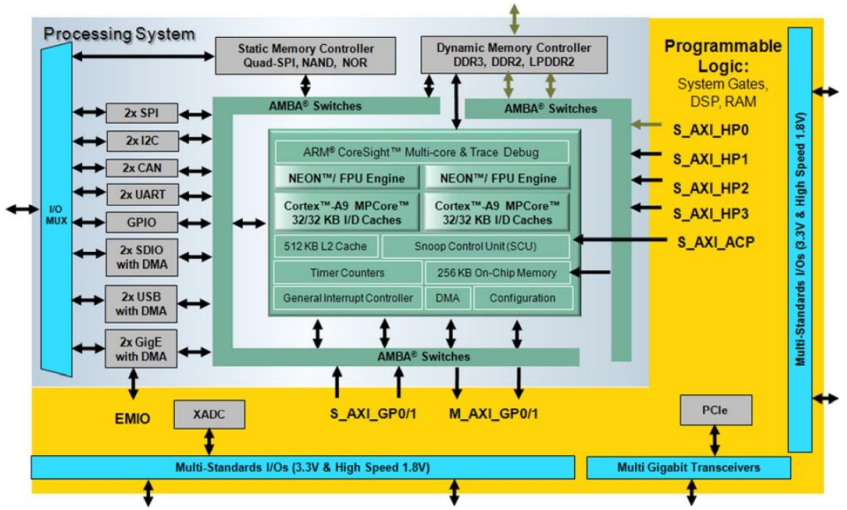
Xilinx Zynq and Zedboard





		Cost-Optimized Devices					Mid-Range Devices			
	Device Name	Z-7007S	Z-7012S	Z-7014S	Z-7010	Z-7015	Z-7020	Z-7030	Z-7035	Z-7045	Z-7100
	Part Number	XC7Z007S	XC7Z012S	XC7Z014S	XC7Z010	XC7Z015	XC7Z020	XC7Z030	XC7Z035	XC7Z045	XC7Z100
Processing System (PS)	Processor Core	Single-Core ARM® Cortex™-A9 MPCore™ Up to 766MHz			Dual-Core ARM Cortex-A9 MPCore Up to 866MHz			Dual-Core ARM Cortex-A9 MPCore Up to 1GHz[1]			
	Processor Extensions	NEON™ SIMD Engine and Single/Double Precision Floating Point Unit per processor									
	L1 Cache	32KB Instruction, 32KB Data per processor									
	L2 Cache	512KB									
	On-Chip Memory	256KB									
	External Memory Support[2]	DDR3, DDR3L, DDR2, LPDDR2									
	External Static Memory Support[2]	2x Quad-SPI, NAND, NOR									
	DMA Channels	8 (4 dedicated to PL)									
	Peripherals	2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO									
	Peripherals w/ built-in DMA[2]	2x USB 2.0 (OTG), 2x tri-mode Gigabit Ethernet, 2x SD/SDIO									
	Security[3]	RSA Authentication of First Stage Boot Loader, AES and SHA 256b Decryption and Authentication for Secure Boot									
	Processing System to Programmable Logic Interface Ports (Primary Interfaces & Interrupts Only)	2x AXI 32b Master, 2x AXI 32b Slave 4x AXI 64b/32b Memory AXI 64b ACP 16 Interrupts									
Programmable Logic (PL)	7 Series PL Equivalent	Artix-7	Artix-7	Artix-7	Artix-7	Artix-7	Artix-7	Kintex-7	Kintex-7	Kintex-7	Kintex-7
	Logic Cells	23K	55K	65K	28K	74K	85K	125K	275K	350K	444K
	Look-Up Tables (LUTs)	14,400	34,400	40,600	17,600	46,200	53,200	78,600	171,900	218,600	277,400
	Flip-Flops	28,800	68,800	81,200	35,200	92,400	106,400	157,200	343,800	437,200	554,800
	Total Block RAM (# 36Kb Blocks)	1.8Mb (50)	2.5Mb (72)	3.8Mb (107)	2.1Mb (60)	3.3Mb (95)	4.9Mb (140)	9.3Mb (265)	17.6Mb (500)	19.2Mb (545)	26.5Mb (755)
	DSP Slices	66	120	170	80	160	220	400	900	900	2,020
	PCI Express	—	Gen2 x4	—	—	Gen2 x4	—	Gen2 x4	Gen2 x8	Gen2 x8	Gen2 x8
	Analog Mixed Signal (AMS) / XADC[2]	2x 12 bit, MSPS ADCs with up to 17 Differential Inputs									
	Security[3]	AES & SHA 256b Decryption & Authentication for Secure Programmable Logic Config									
	Speed Grades Commercial	-1			-1			-1			-1
	Speed Grades Extended	-2			-2,-3			-2,-3			-2
	Speed Grades Industrial	-1, -2			-1, -2, -3			-1, -2, -2L			-1, -2, -2L

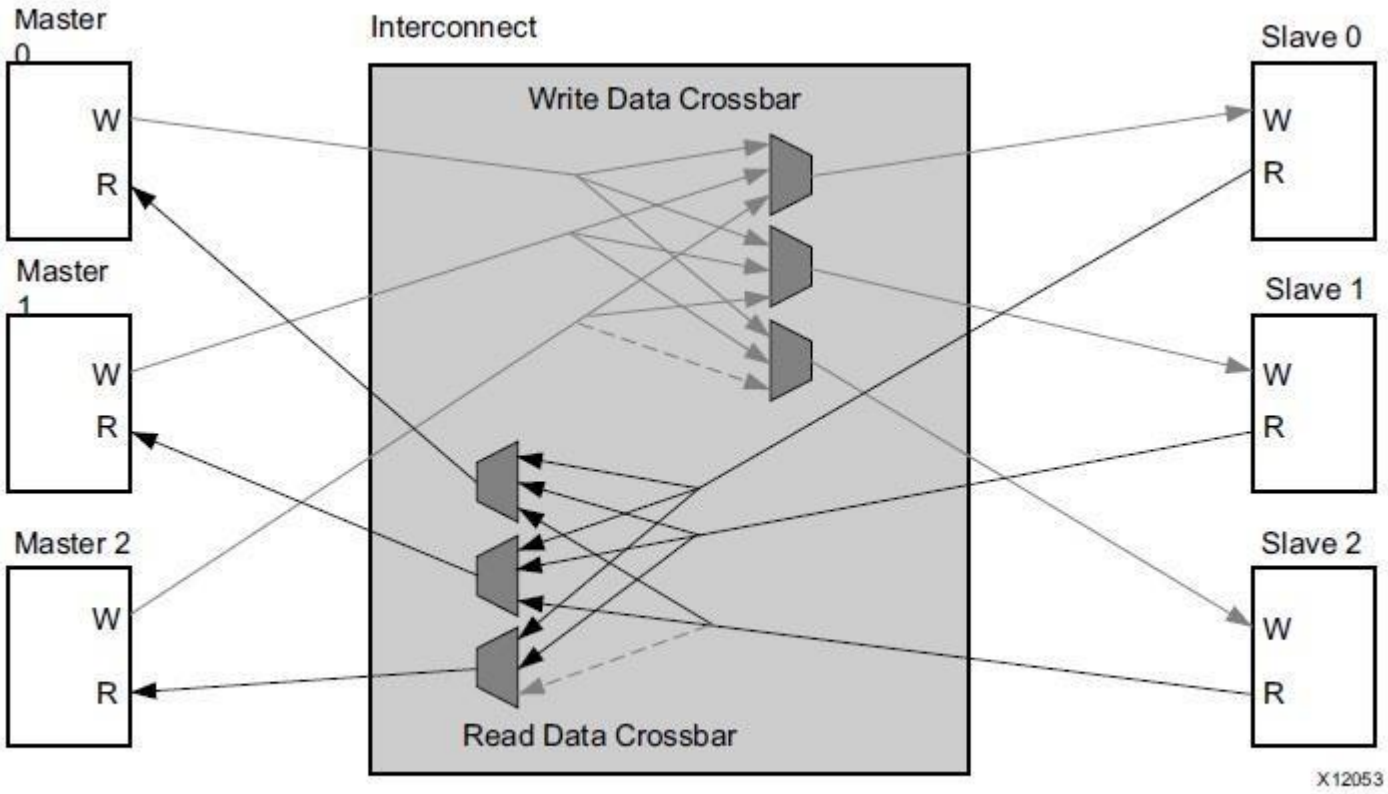
Zynq-7000 SoC Block Diagram



ENSTA
IP PARIS

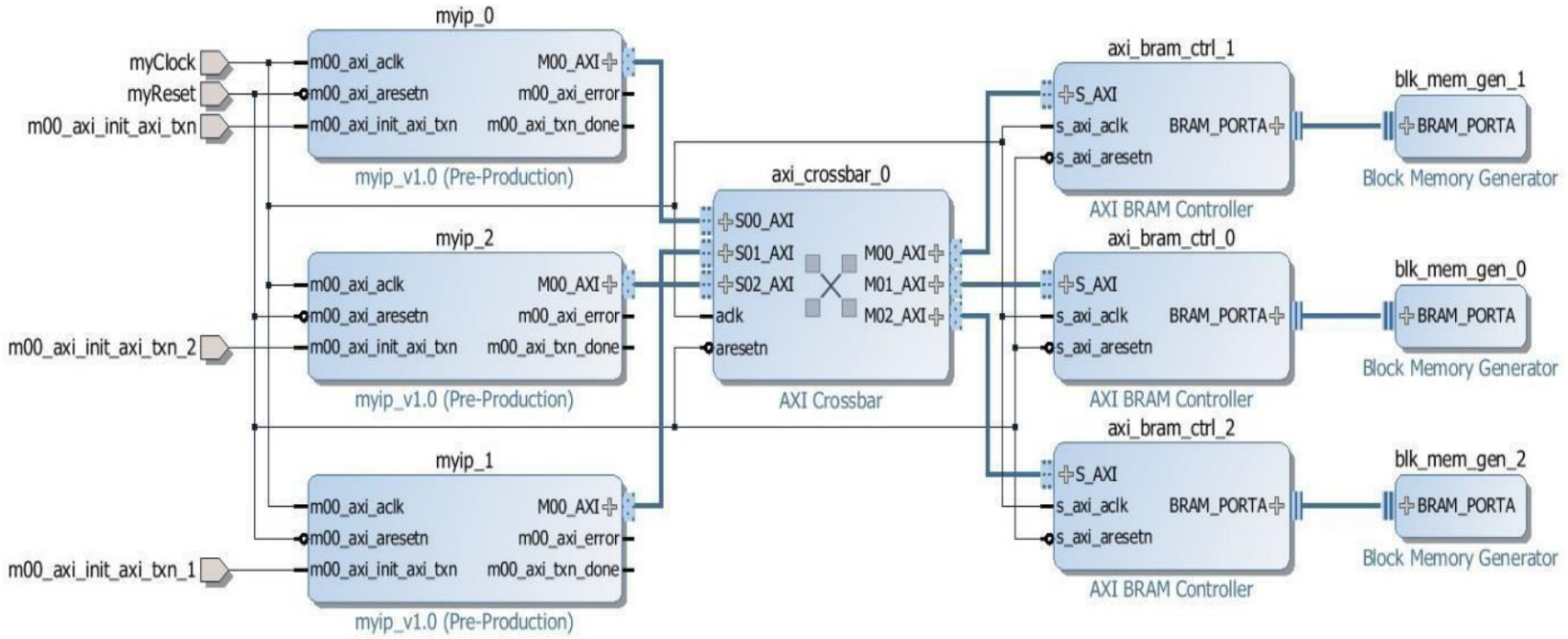
Multicore

AXI Crossbar



Sparse Crossbar Write and Read Data Pathways

Q1. Network on chip (NOC) 3x3

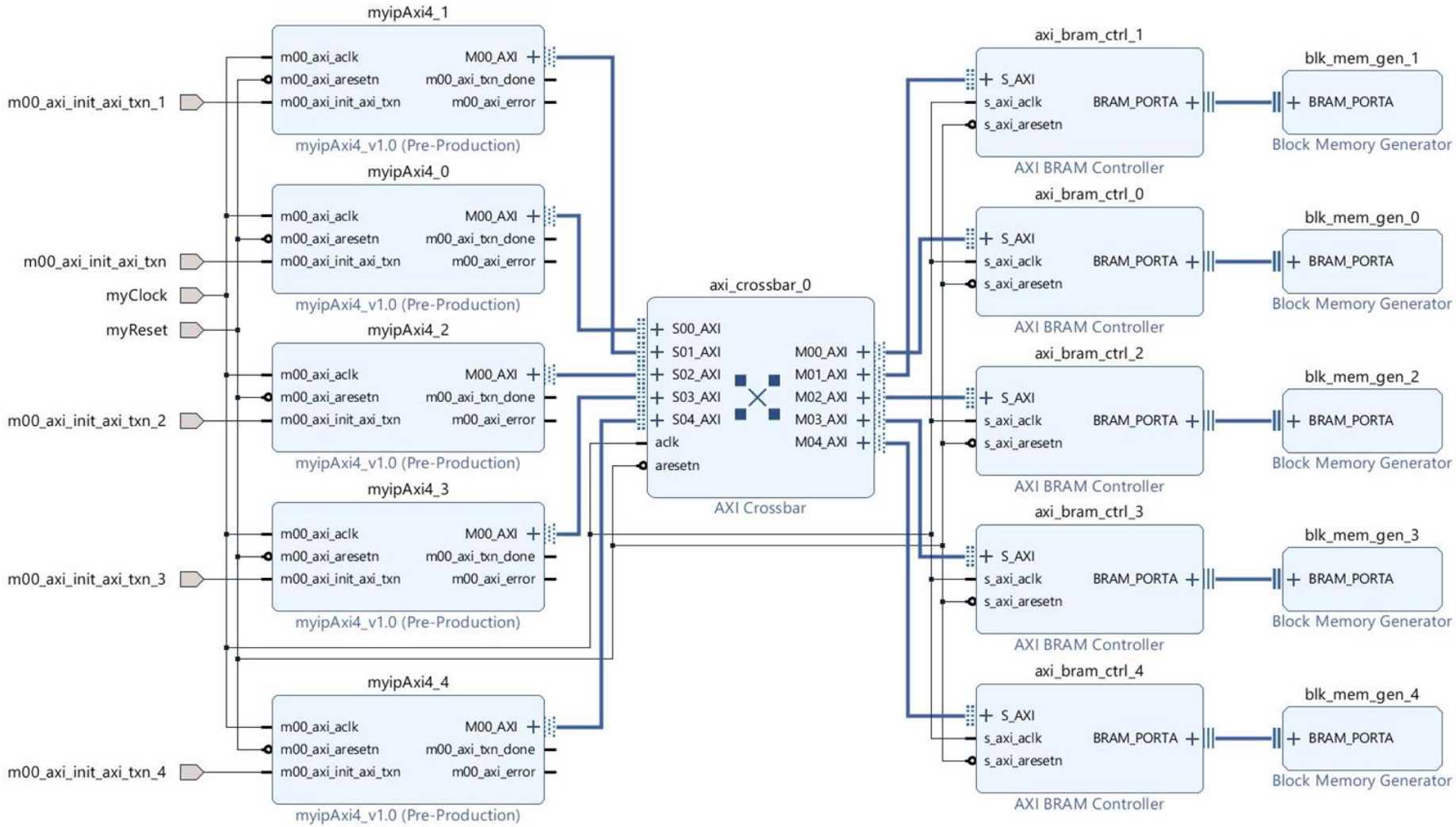


Exemple:
https://drive.google.com/drive/folders/1MIse0ENNUip1Cd_axxJYRaN9nohlsSbK?usp=sharing

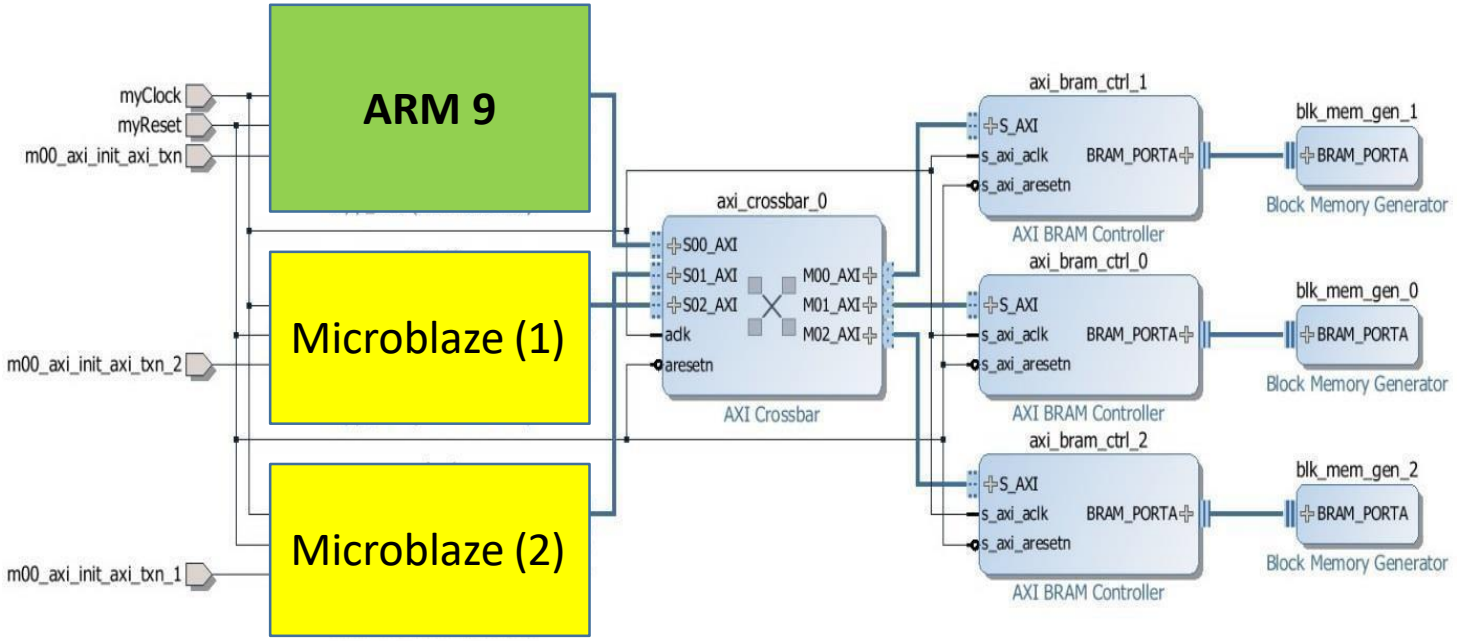
Q1. Network on chip (NOC) 3x3

- Q1.1 NOC Design and latency/bandwith analysis through simulation
- Q1.2 NOC implementation on Zynq and Board execution – Explore NOC options
- Q1.3 NOC Place and route improvements
- Q1.4 Test and validation on zedboard.

  - AXI Traffic Generator v3.0 LogiCORE IP Product Guide Vivado Design Suite PG125 February 11, 2019
  - AXI Interconnect v2.1 LogiCORE IP Product Guide Vivado Design Suite PG059 Dec. 20, 2017

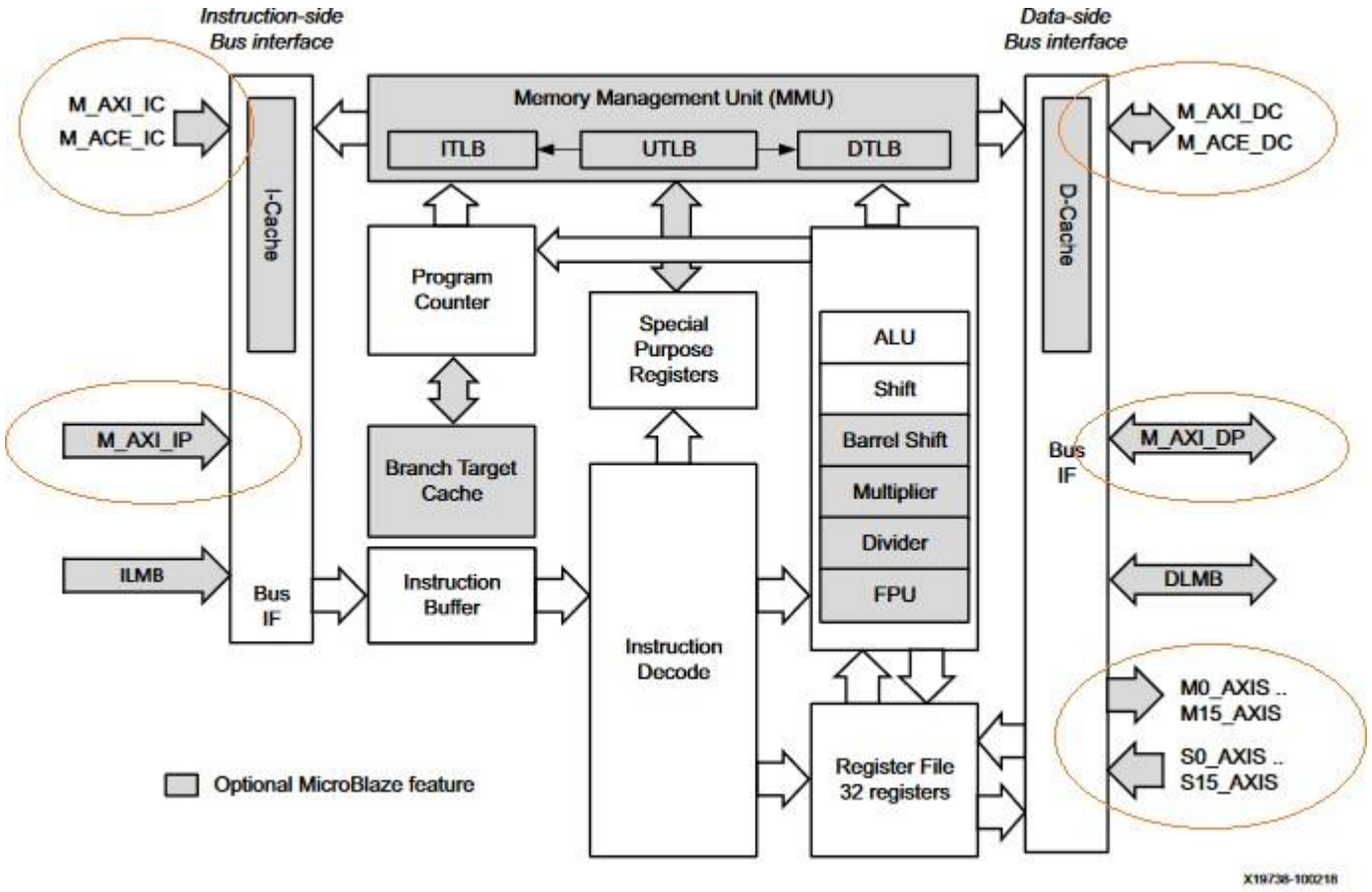

myipAxi4_1
m00_axi_aclk
m00_axi_aresetn
m00_axi_init_axi_txn
M00_AXI
m00_axi_txn_done
m00_axi_error
myipAxi4_v1.0 (Pre-Production)
m00_axi_init_axi_txn_1
myipAxi4_0
m00_axi_init_axi_txn
myipAxi4_v1.0 (Pre-Production)
myClock
myReset
myipAxi4_2
m00_axi_init_axi_txn_2
myipAxi4_v1.0 (Pre-Production)
myipAxi4_3
m00_axi_init_axi_txn_3
myipAxi4_v1.0 (Pre-Production)
myipAxi4_4
m00_axi_init_axi_txn_4
myipAxi4_v1.0 (Pre-Production)
axi_crossbar_0
S00_AXI
S01_AXI
S02_AXI
S03_AXI
S04_AXI
aclk
aresetn
M00_AXI
M01_AXI
M02_AXI
M03_AXI
M04_AXI
AXI Crossbar
axi_bram_ctrl_1
S_AXI
s_axi_aclk
s_axi_aresetn
BRAM_PORTA
AXI BRAM Controller
blk_mem_gen_1
BRAM_PORTA
Block Memory Generator
axi_bram_ctrl_0
AXI BRAM Controller
blk_mem_gen_0
Block Memory Generator
axi_bram_ctrl_2
AXI BRAM Controller
blk_mem_gen_2
Block Memory Generator
axi_bram_ctrl_3
AXI BRAM Controller
blk_mem_gen_3
Block Memory Generator
axi_bram_ctrl_4
AXI BRAM Controller
blk_mem_gen_4
Block Memory Generator

Q2. Multicore 3 cores : 1 ARM 2 Microblaze v.1



https://www.xilinx.com/support/documentation/sw_manuals/xilinx2019_2/ug984-vivado-microblaze-ref.pdf

Q2. Multicore 3 cores : 1 ARM 2 Microblaze customization



MicroBlaze Core Block Diagram

Microblaze interface signals

- **M_AXI_DP:** Peripheral Data Interface, AXI4-Lite or AXI4 interface
- **M_AXI_IP:** Peripheral Instruction interface, AXI4-Lite interface

- **M0_AXIS..M15_AXIS:** AXI4-Stream interface master direct connection interfaces
- **S0_AXIS..S15_AXIS:** AXI4-Stream interface slave direct connection interfaces
- **M_AXI_DC:** Data-side cache AXI4 interface
- **M_ACE_DC:** Data-side cache AXI Coherency Extension (ACE) interface
- **M_AXI_IC:** Instruction-side cache AXI4 interface
- **M_ACE_IC:** Instruction-side cache AXI Coherency Extension (ACE) interface
- **Core: Miscellaneous signals for: clock, reset, interrupt, debug, trace**
- **ILMB:** Instruction interface, Local Memory Bus (BRAM only)
- **DLMB:** Data interface, Local Memory Bus (BRAM only)

Q2. Multicore 3 cores : 1 ARM 2 Microblaze

- Q2.3 synthesis place and route multicore frequency ?
- Q2.4 clock frequencies – multi-clock

Configurations Microblaze (1/3)

Table 2-1: **Configurable Feature Overview by MicroBlaze Version**

Feature	MicroBlaze versions					
	v9.3	**v9.4**	**v9.5**	**v9.6**	**v10.0**	**v11.0**
Version Status	deprecated	deprecated	deprecated	deprecated	deprecated	preferred
Processor pipeline depth	3/5	3/5	3/5	3/5	3/5/8	3/5/8
Local Memory Bus (LMB) data side interface	option	option	option	option	option	option
Local Memory Bus (LMB) instruction side interface	option	option	option	option	option	option
Hardware barrel shifter	option	option	option	option	option	option
Hardware divider	option	option	option	option	option	option
Hardware debug logic	option	option	option	option	option	option
Stream link interfaces	0-16 AXI	0-16 AXI	0-16 AXI	0-16 AXI	0-16 AXI	0-16 AXI
Machine status set and clear instructions	option	option	option	option	option	option
Cache line word length	4, 8	4, 8	4, 8, 16	4, 8, 16	4, 8, 16	4, 8, 16
Hardware exception support	option	option	option	option	option	option
Pattern compare instructions	option	option	option	option	option	option
Floating-point unit (FPU)	option	option	option	option	option	option

Configurations Microblaze (2/3)

Table 2-1: **Configurable Feature Overview by MicroBlaze Version *(Cont'd)***

Feature	MicroBlaze versions					
	v9.3	v9.4	v9.5	v9.6	v10.0	v11.0
Disable hardware multiplier[1]	option	option	option	option	option	option
Hardware debug readable ESR and EAR	Yes	Yes	Yes	Yes	Yes	Yes
Processor Version Register (PVR)	option	option	option	option	option	option
Area or speed optimized	option	option	option	option	option	option
Hardware multiplier 64-bit result	option	option	option	option	option	option
LUT cache memory	option	option	option	option	option	option
Floating-point conversion and square root instructions	option	option	option	option	option	option
Memory Management Unit (MMU)	option	option	option	option	option	option
Extended stream instructions	option	option	option	option	option	option
Use Cache Interface for All I-Cache Memory Accesses	option	option	option	option	option	option
Use Cache Interface for All D-Cache Memory Accesses	option	option	option	option	option	option
Use Write-back Caching Policy for D-Cache	option	option	option	option	option	option
Branch Target Cache (BTC)	option	option	option	option	option	option

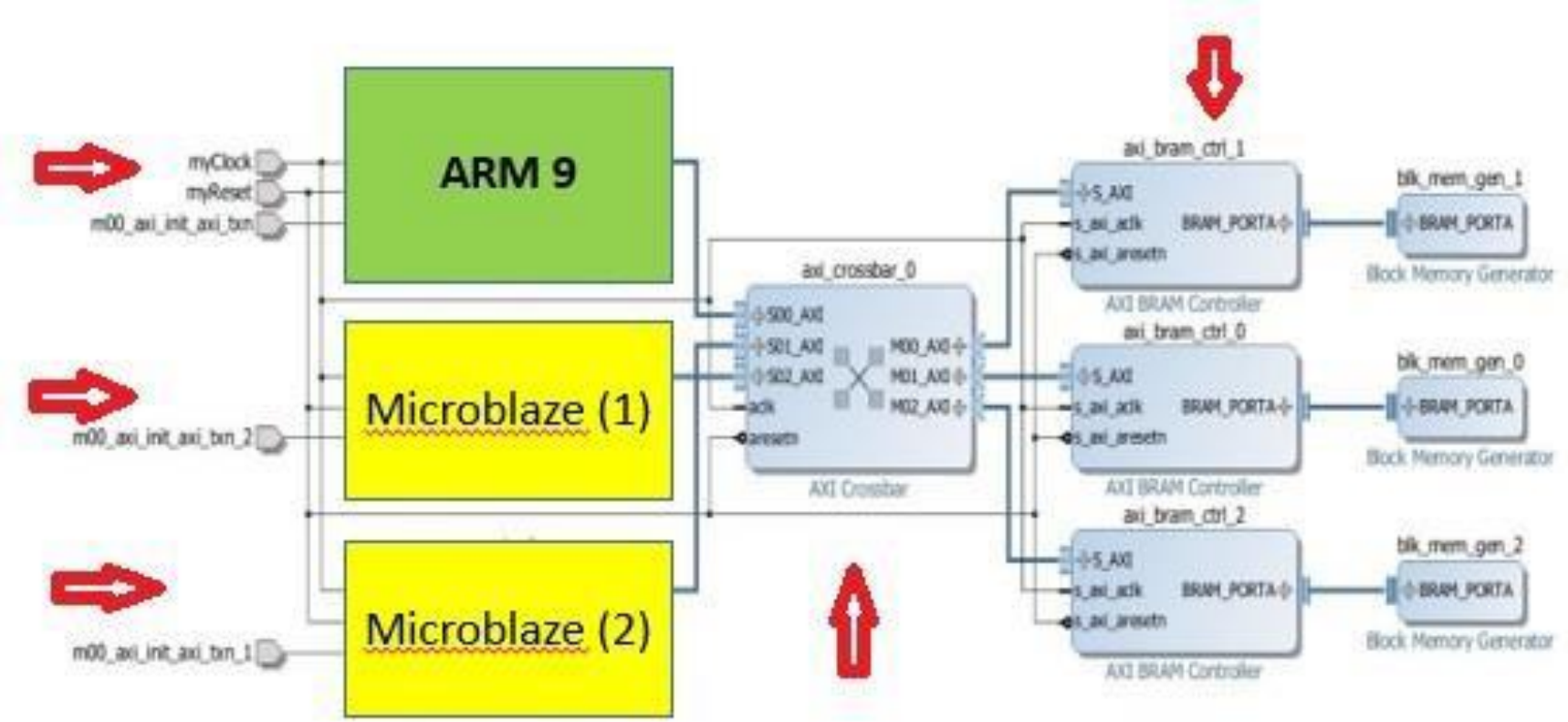
Configurations Microblaze (3/3)

Streams for I-Cache	option	option	option	option	option	option
Victim handling for I-Cache	option	option	option	option	option	option
Victim handling for D-Cache	option	option	option	option	option	option
AXI4 (M_AXI_DP) data side interface	option	option	option	option	option	option
AXI4 (M_AXI_IP) instruction side interface	option	option	option	option	option	option
AXI4 (M_AXI_DC) protocol for D-Cache	option	option	option	option	option	option
AXI4 (M_AXI_IC) protocol for I-Cache	option	option	option	option	option	option
AXI4 protocol for stream accesses	option	option	option	option	option	option
Fault tolerant features	option	option	option	option	option	option
Force distributed RAM for cache tags	option	option	option	option	option	option
Configurable cache data widths	option	option	option	option	option	option
Count Leading Zeros instruction	option	option	option	option	option	option
Memory Barrier instruction	Yes	Yes	Yes	Yes	Yes	Yes
Stack overflow and underflow detection	option	option	option	option	option	option
Allow stream instructions in user mode	option	option	option	option	option	option

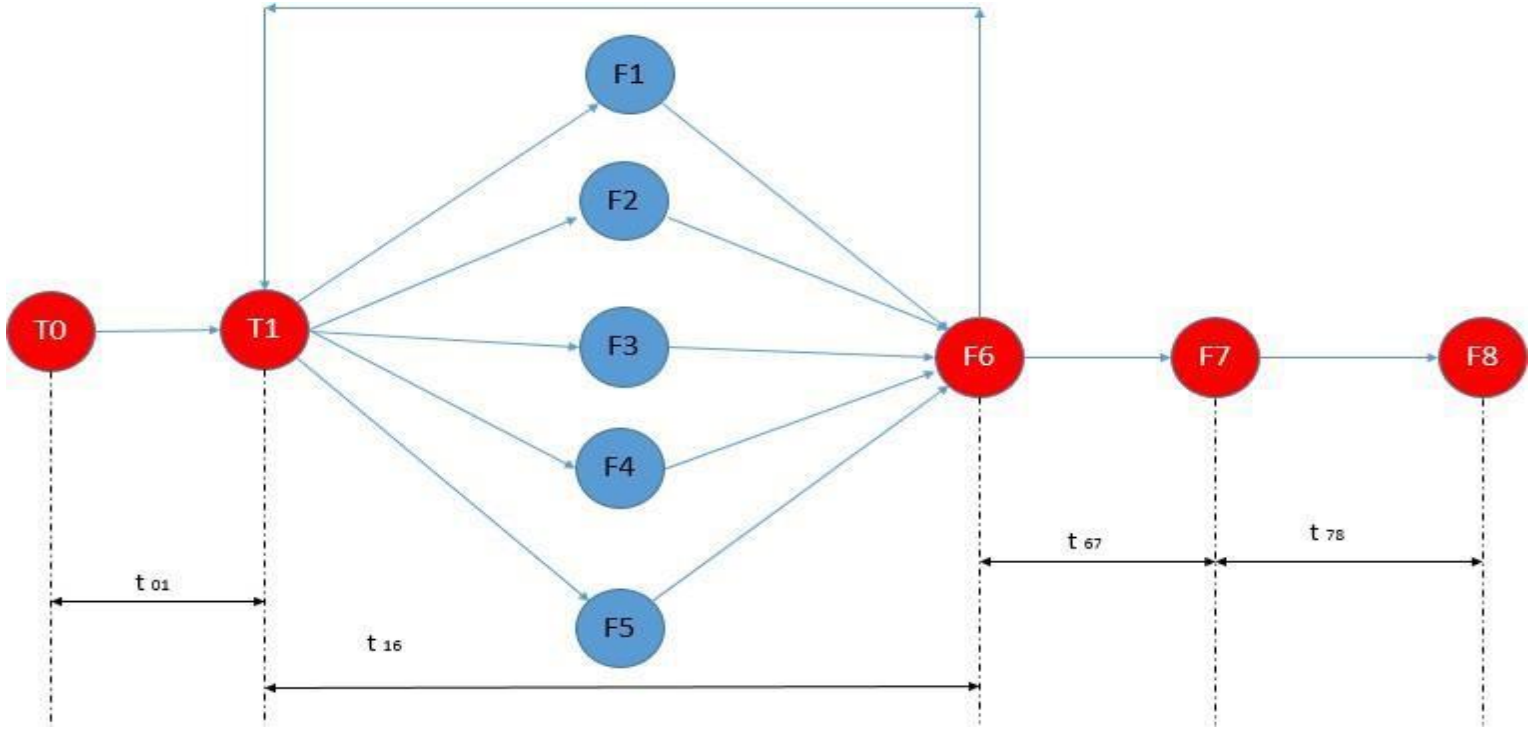
Q2. Multicore 3 cores : 1 ARM 2 Microblaze

- Q2.4 Explorations options Microblaze: *(Barrel shifter, multiplier, divider, FPU, BTC, Icache, Dcache)*
- synthesis place and route multicore DSE

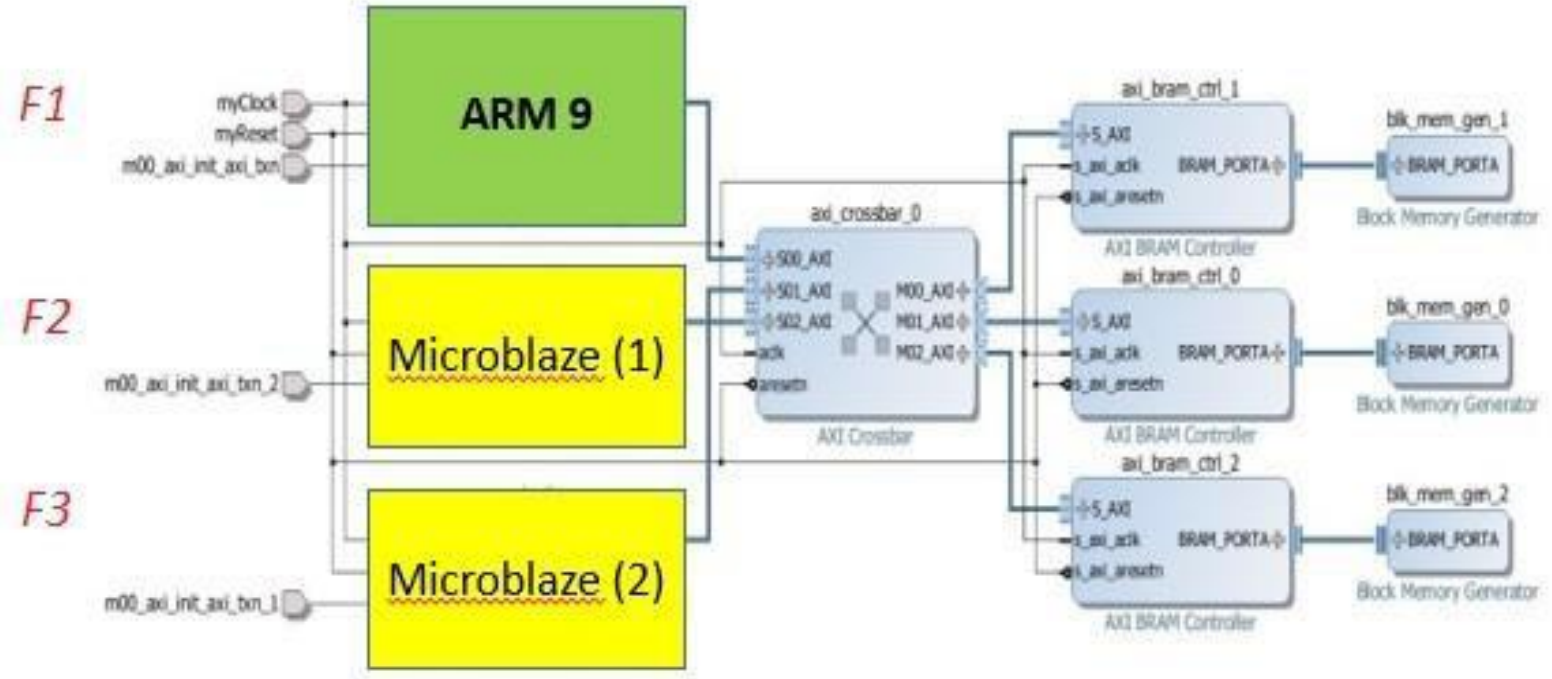
Multicore multi-clock



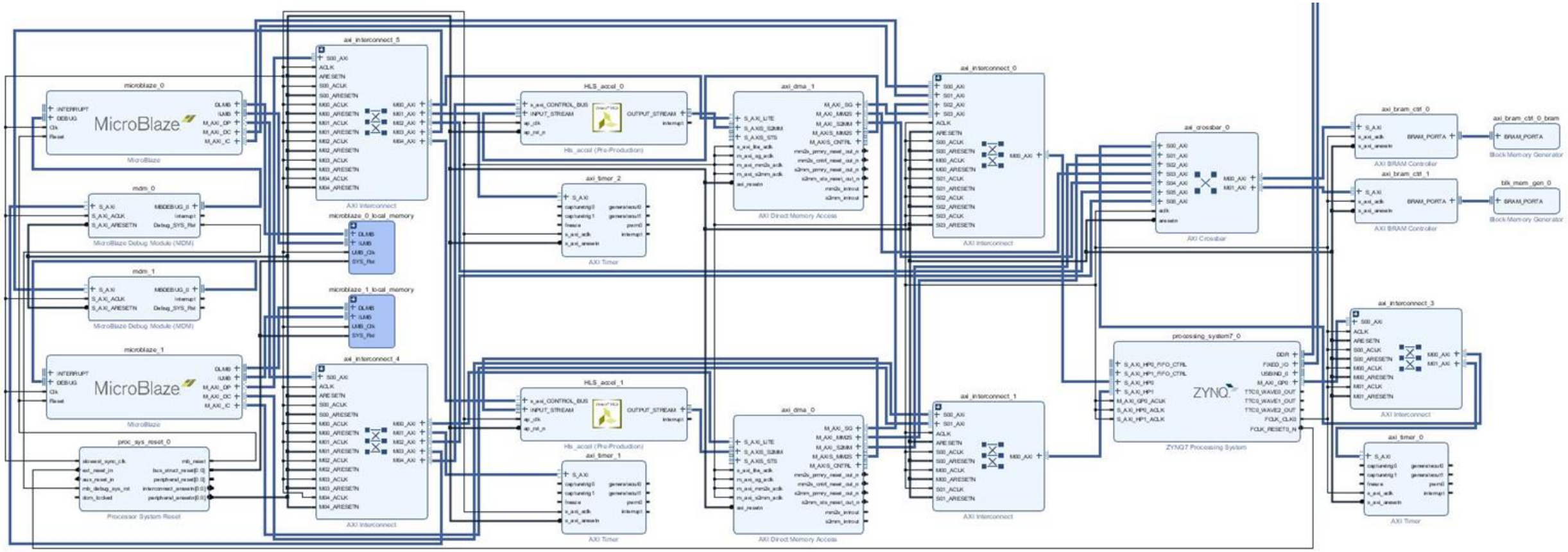
Q3. programming Application



3 programs F1, F2 et F3 executing separetly



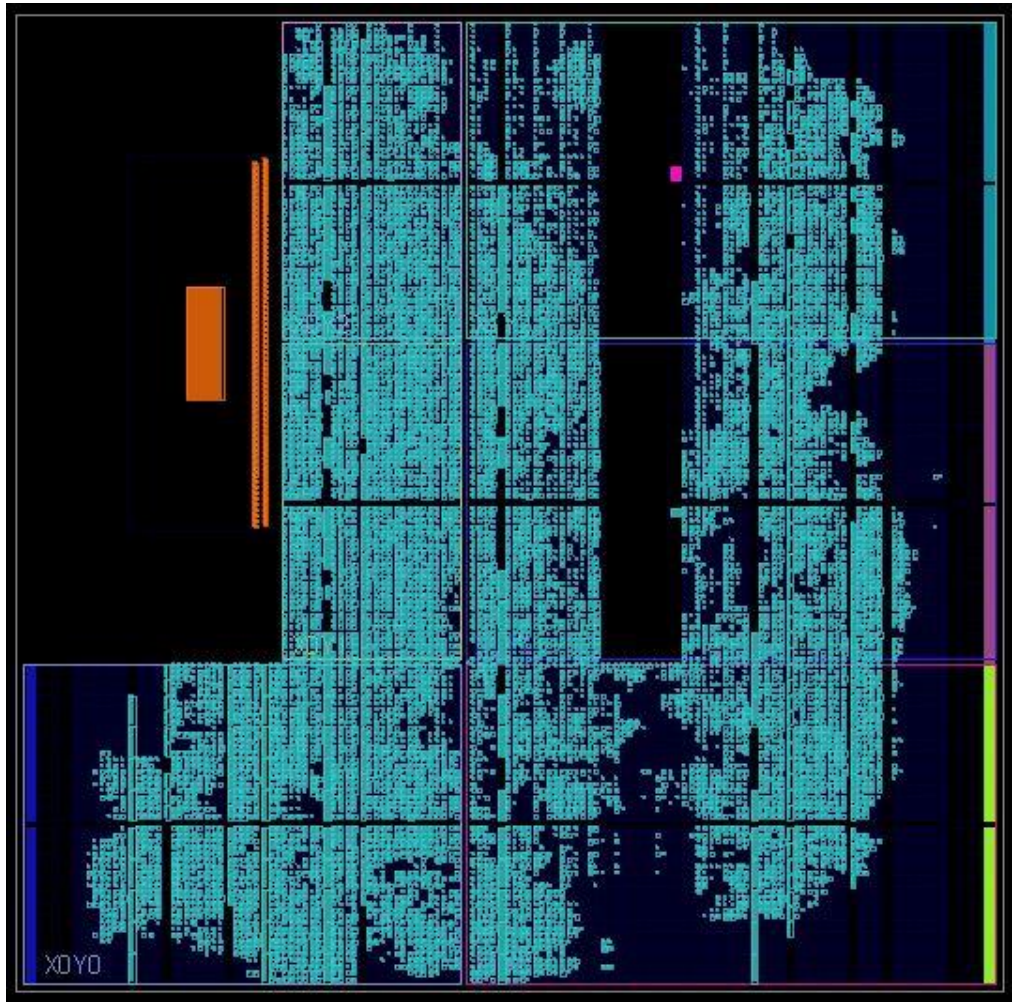
Ips integration

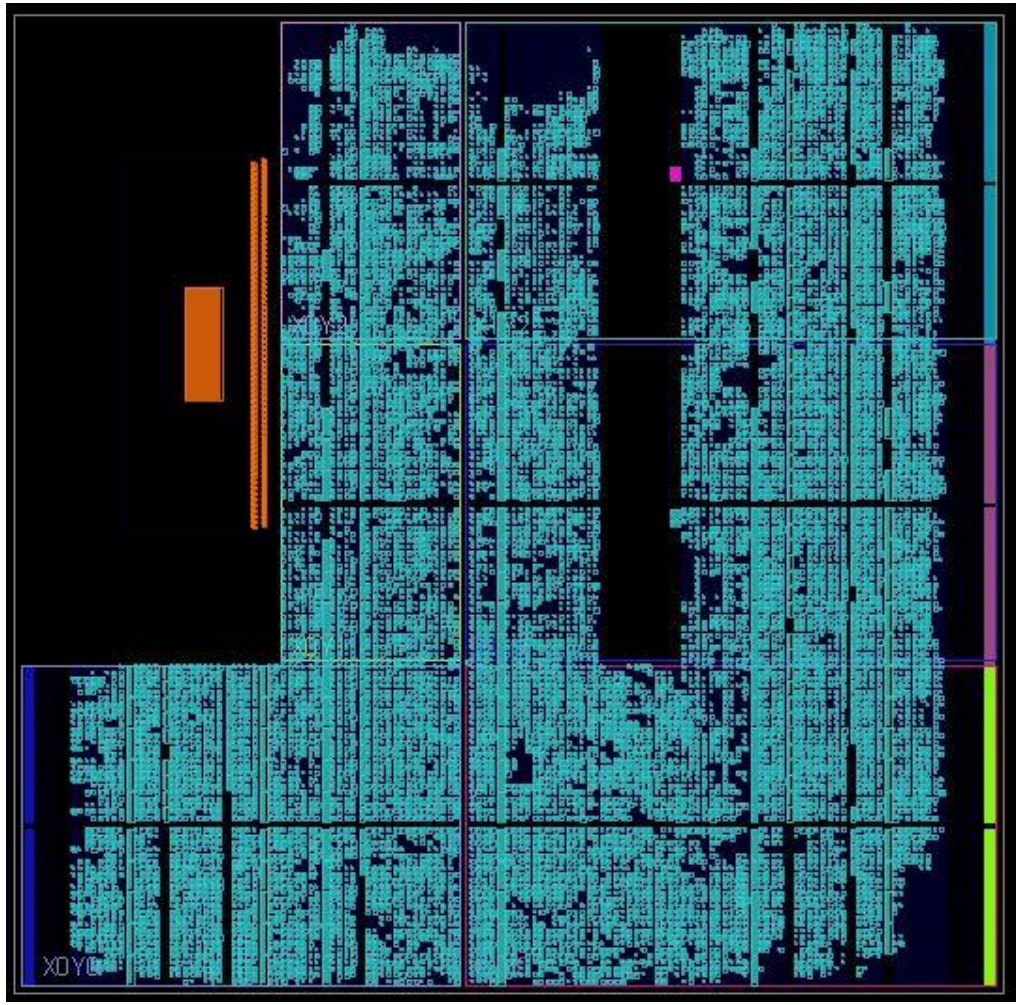


Place Design (11 errors)

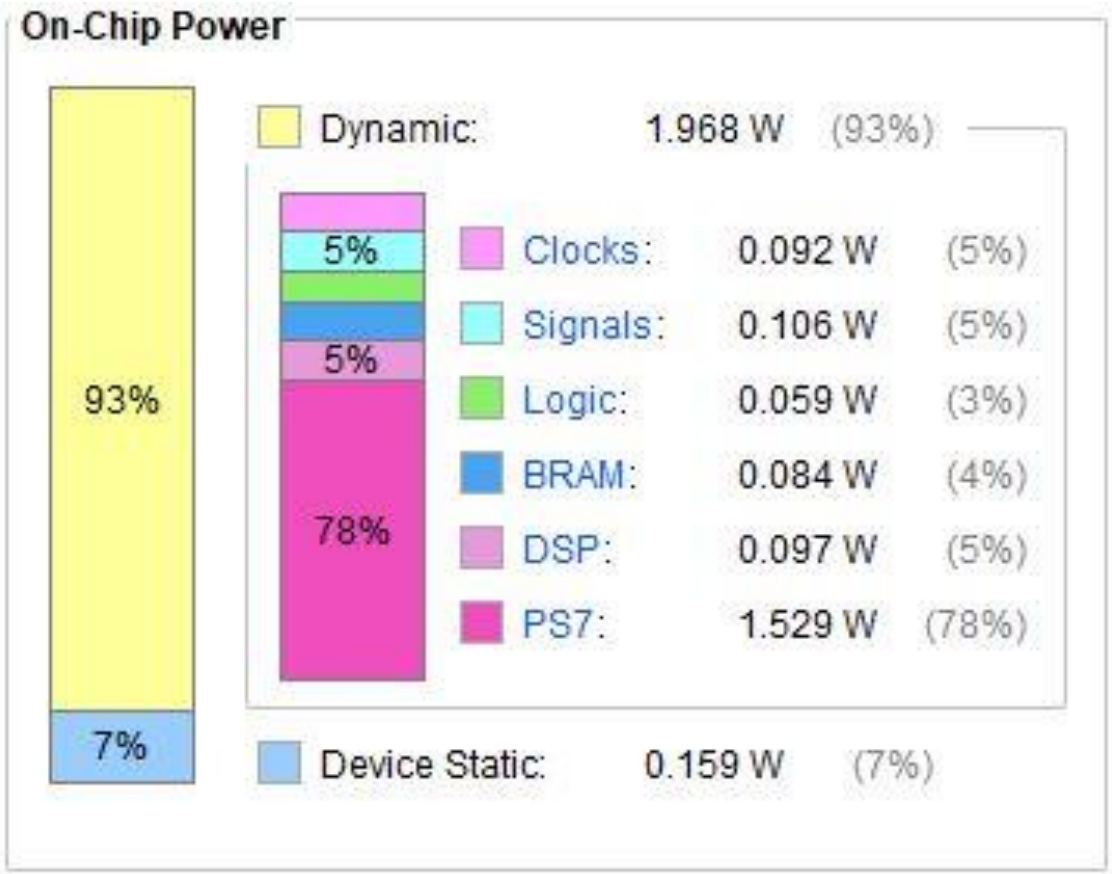
[Place 30-640] Place Check : This design requires more Slice LUTs cells than are available in the target device. This design requires 77466 of such cell types but only 53200 compatible sites are available in the target device. Please analyze your synthesis results and constraints to ensure the design is mapped to Xilinx primitives as expected. If so, please consider targeting a larger device. Please set tcl parameter "drc.disableLUTOverUtilError" to 1 to change this error to warning. (8 more like this)

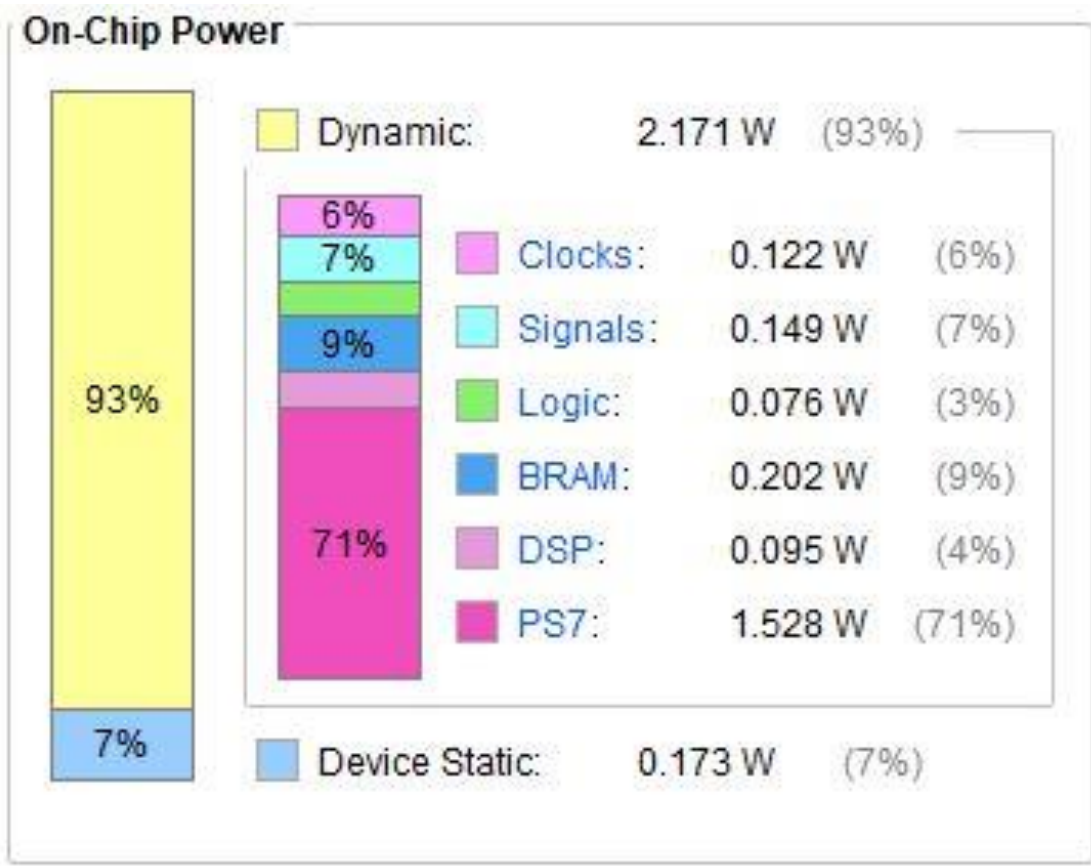
Chip Area



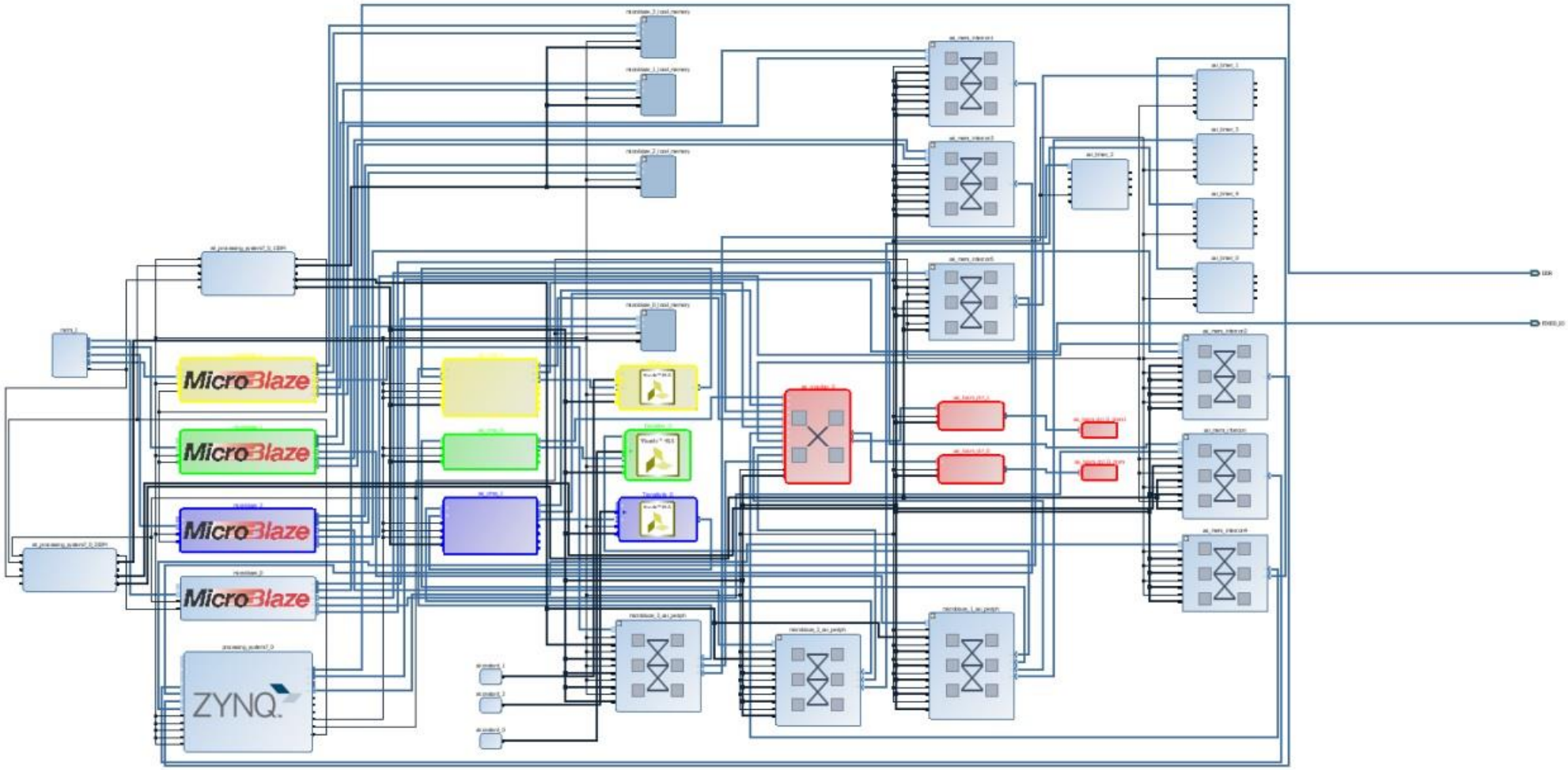


Power


On-Chip Power
93%
7%
Dynamic: 1.968 W (93%)
5%
5%
78%
Clocks: 0.092 W (5%)
Signals: 0.106 W (5%)
Logic: 0.059 W (3%)
BRAM: 0.084 W (4%)
DSP: 0.097 W (5%)
PS7: 1.529 W (78%)
Device Static: 0.159 W (7%)


On-Chip Power
93%
7%
Dynamic: 2.171 W (93%)
6%
7%
9%
71%
Clocks: 0.122 W (6%)
Signals: 0.149 W (7%)
Logic: 0.076 W (3%)
BRAM: 0.202 W (9%)
DSP: 0.095 W (4%)
PS7: 1.528 W (71%)
Device Static: 0.173 W (7%)

Heterogeneous Embedded Multicore : ARM9 (dual core) + 4 MB Embedded Processor with NOC and Hardware accelerators



Conclusion and perspectives

- A intensive course on embedded systems and heterogeneous embedded multicore
- Highly appreciated by industry partners (ARM, Qualcomm, etc…)
- Skills mastering and understanding confirmed over the years
- Quality projects and strong investments from ENSTA students
- Tools learning curves an issue and increasingly complex and memory demanding (students laptop issues)
- Online supports a must with projects sharing through collaborative platforms (drive,etc…)
- **No Black-Box design :** down to synthesis place and route implementation

Conclusion and perspectives

- **Objectives on FPGA Platforms (Xilinx)** :
  1. design, implementation and optimization of complex embedded systems
  2. discover, understand and master potentials of FPGA Technology
  3. design of hardware accelerators under energy/area/performance constraints
  4. design of embedded multicore with emphasis on NOCs (Network on Chips)
  5. Parallel programming
  6. Automatic Design Space Exploration and MDAO
- Objectives reached and in evolution

Robot Clearpath Robotics – Husky

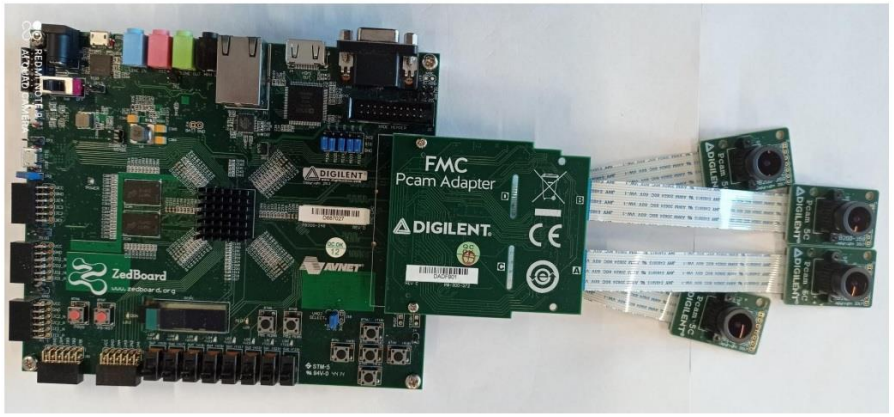
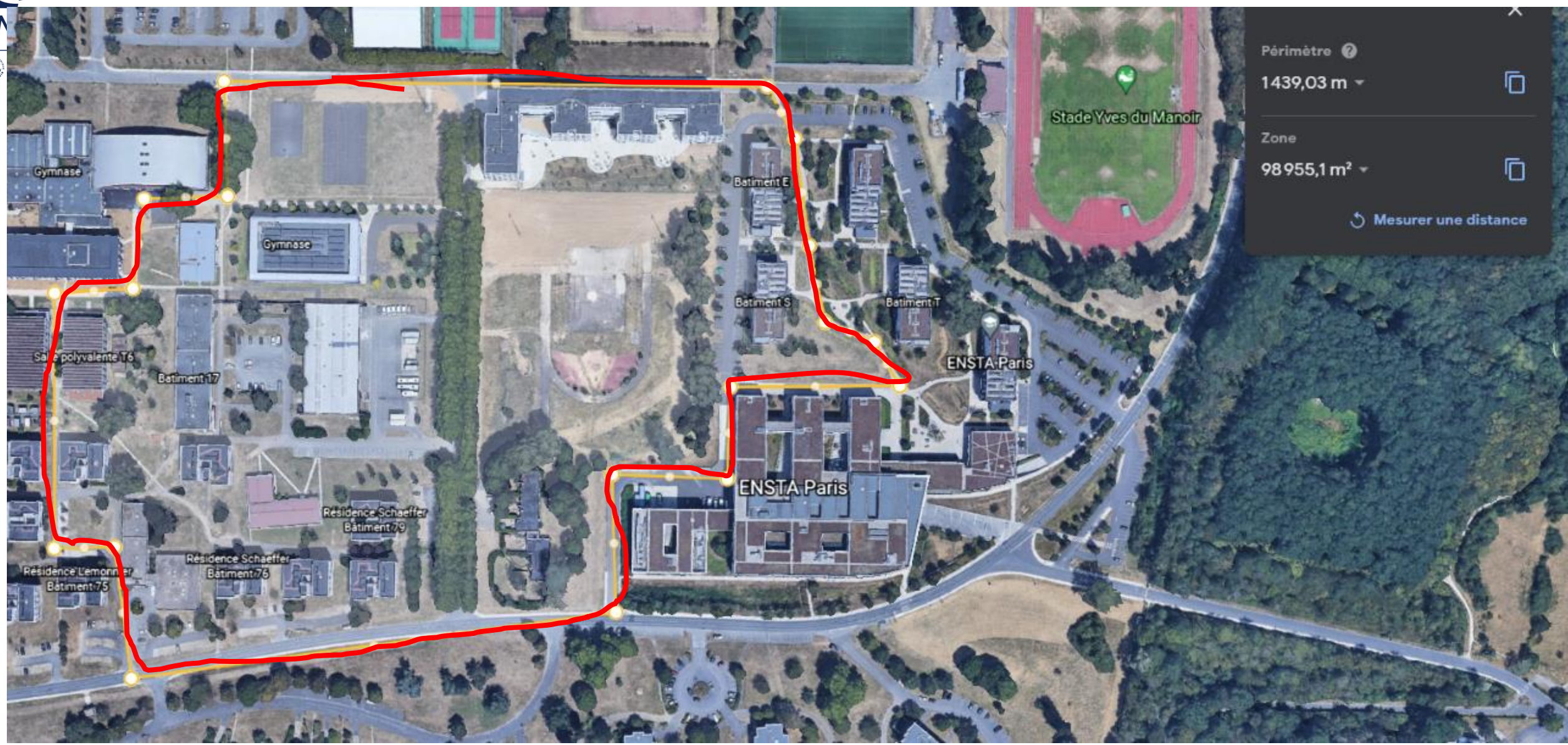


Image processing and vision
Path planning and obstacle avoidance
Autonomous robotics

Réference : https://clearpathrobotics.com/


Périmètre
1439,03 m
Zone
98 955,1 m²
Mesurer une distance
Stade Yves du Manoir
Gymnase
Gymnase
Batiment E
Batiment S
Batiment T
ENSTA Paris
Salle polyvalente T6
Batiment 17
ENSTA Paris
Résidence Schaeffer
Batiment 79
Résidence Schaeffer
Batiment 76
Résidence Lemonnier
Batiment 75

Thanks to our partners and contributors

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ARTERIS IP Qualcomm SIPEARL


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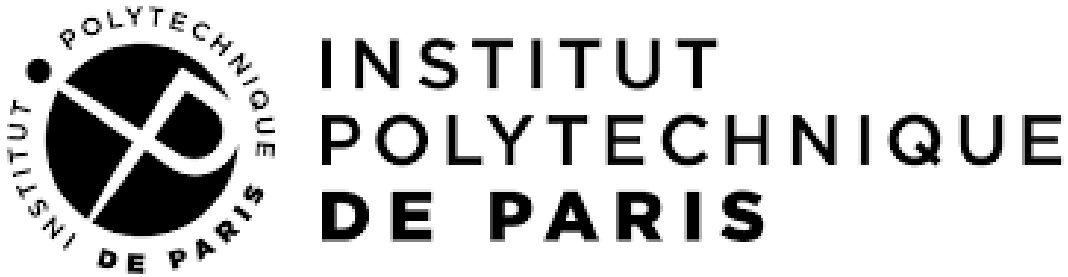
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