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# Heterogeneous Embedded Multicore Design Graduate Education in ENSTA PARIS: A 5 years Feedback

*jeudi 7 juillet 2022 11:45 (45 minutes)*

In this talk we will present a 5 years feedback on training graduate level students in the oldest school of engineers in France, ENSTA PARIS on heterogeneous embedded multicore design on Xilinx SOC Zynq chip. Part of the ROB 307 MPSOC (Multiprocessor System on Chip) course students are required to design a Heterogeneous Embedded Multicore combining a dual core hardcore IP (ARM9, 4 soft cores Microblaze, 2 hardware accelerators (Neural network, vision, image processing) and a AXI NOC (Network on Chip) on a single Zynq XC7Z020 chip using a zedboard. Students are expected to validate their design through actual execution on the zedboard and have all IPs running concurrently. This project have been going on for the past 5 yeat and we will share our experience in this training.

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