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FPGA acceleration of 3D CT reconstruction using OpenCL and oneAPI Tools

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Many-core processors such as GPUs are currently the preferred technological target for accelerating HPC applications. However, architectures designed on FPGAs can be interesting alternatives to GPUs because they are potentially lower power and accessible thanks to the new high-level synthesis tools (HLS) provided by the leading manufacturers such as Intel or Xilinx. However, exploiting the full potential of FPGAs via HLS tools requires a deep knowledge of their architecture and a significant effort to match the application to the underlying architecture. In this presentation, I will present the principle of HLS tools as well as a methodology for FPGA acceleration through Intel's OpenCL and OneAPI tools. The 3D back-projection operator, present in iterative tomographic reconstruction algorithms, is considered as a use case for this methodology.

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