Scientific Computing Accelerated on FPGA

5 Juillet 2022

Olivier REGNAULT

AVNET SILICA

mardi 05/07	09:00	10:00		**AMD-Xilinx System On Chip (SoC) FPGA, une introduction + démo** Olivier Régnault
	10:00	10:30		Break
	10:30	12:30		**Introduction AMD-XilinX Vitis HLS** William Duluc
	12:30	14:00		Lunch
	14:00	15:30		**Hands-on AMD-XilinX Vitis HLS** William Duluc
	15:30	16:00		Break
	16:00	17:30		**Hands-on AMD-XilinX Vitis HLS** William Duluc

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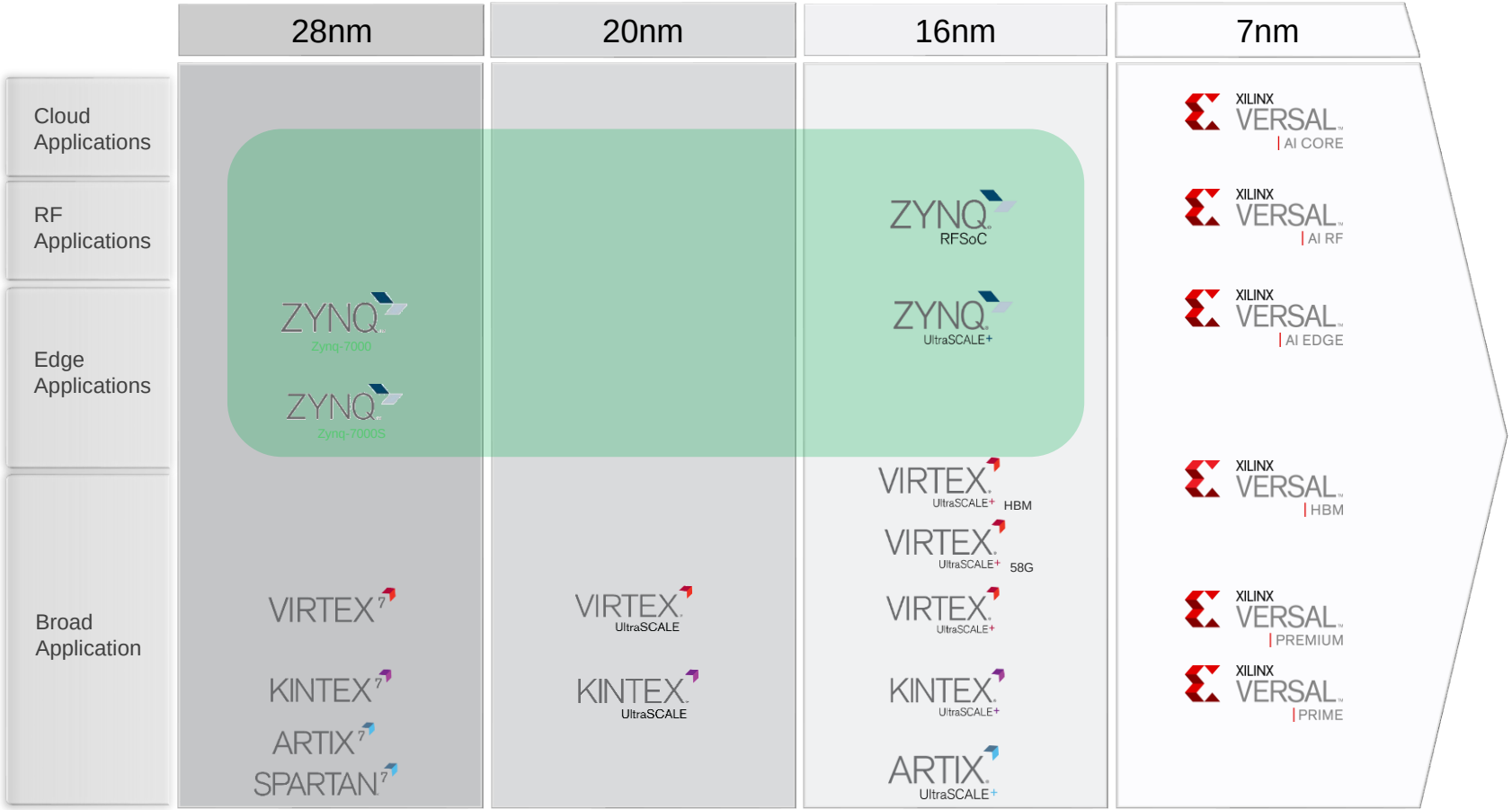
Xilinx Portfolio



16nm UltraScale+ FPGA and MPSoC Scalability

FPGAs

New Cost-Optimized Family

ARTIX UltraSCALE+

- Up to 309K System Logic Cells
- Up to 1,200 DSP Slices
- 16Gb/s Transceivers

Price/Performance/Watt

KINTEX UltraSCALE+

- Up to 1,843K System Logic Cells
- Up to 3,528 DSP Slices
- 32.75Gb/s Transceivers

Highest Performance and Logic Density

VIRTEX UltraSCALE+

- Up to 8,938K System Logic Cells
- Up to 12,288 DSP Slices
- Up to 58Gb/s Transceivers

Zynq UltraScale+ MPSoCs

New ZU1 Device

CG Devices

- **Dual**-Core Arm® Cortex®-A53 up to **1.3GHz**
- Dual-Core Arm Cortex-R5F up to **533MHz**
- Up to 600K System Logic Cells

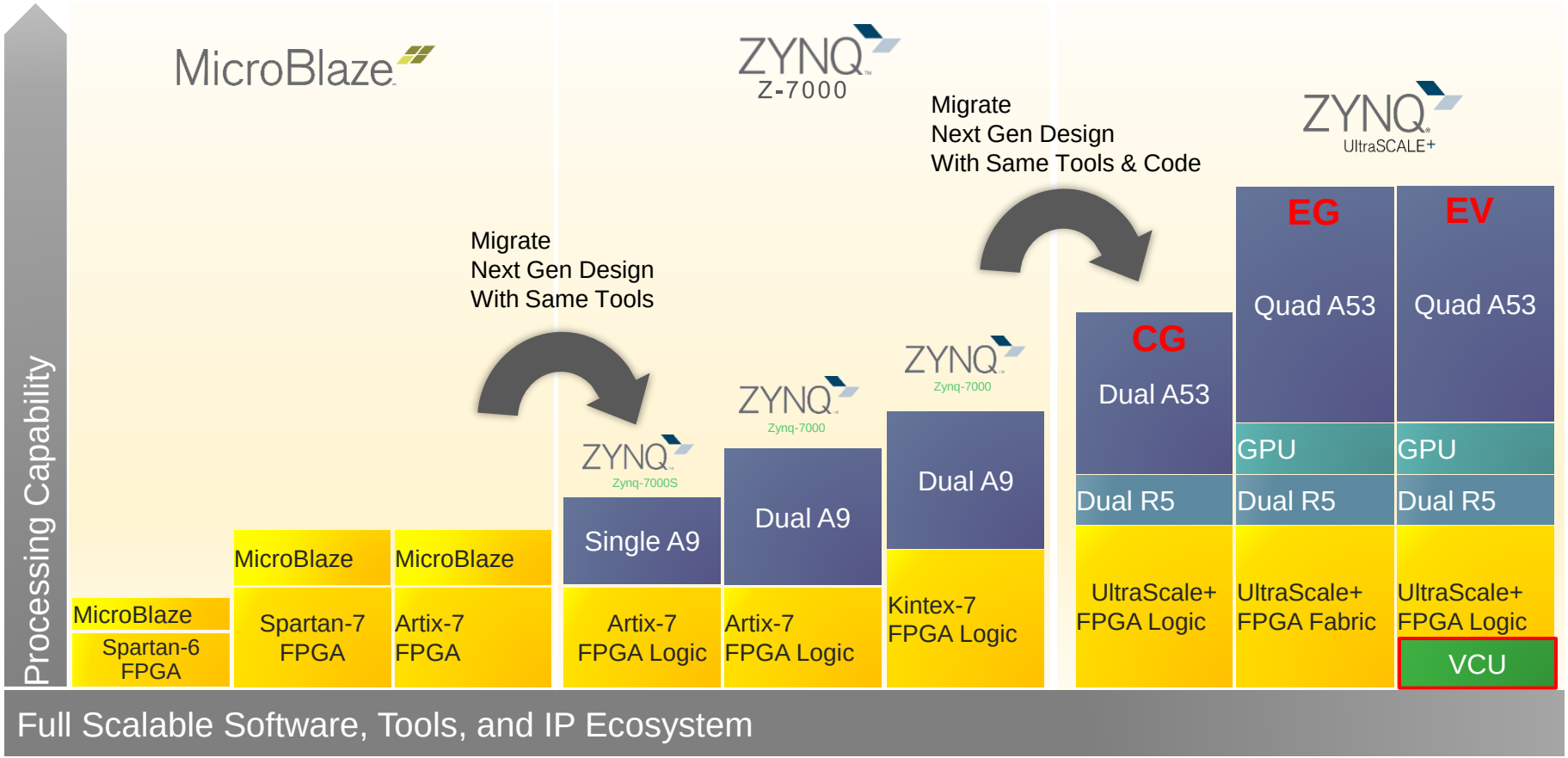
EG Devices

- **Quad**-Core Arm Cortex-A53 up to **1.5GHz**
- Dual-Core Arm Cortex-R5F up to **600MHz**
- Arm Mali™-400MP2 GPU
- Up to 1,143K System Logic Cells

EV Devices

- Quad-Core Arm Cortex-A53 up to 1.5GHz
- Dual-Core Arm Cortex-R5F up to 600MHz
- Arm Mali-400MP2 GPU
- **Video Codec H.264/H.265**
- Up to 504K System Logic Cells

A Broad Range of Processing Performance



Zynq Ultrascale+ MPSoC : Block Diagram

APU : 2 or 4 cores
GPU : with or without
VCU : with or Without

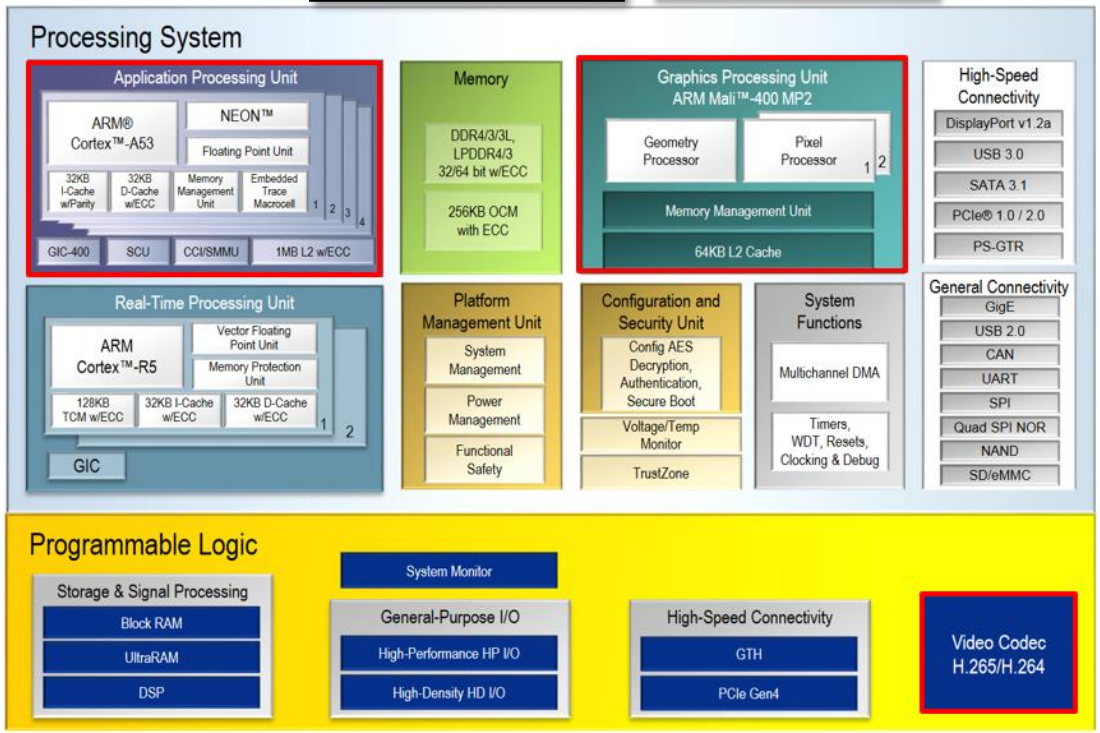
Interface	Max Bandwidth (Mb/s)
DDR4	2400*
LPDDR4	2400
DDR3	2133
DDR3L	1866
LPDDR3	1800

*DDR4 up to 2,667Mb/s in Programmable Logic

ARM Mali™-400 MP2
up to 667MHz
- Full HD Support (1080p)
- 2D & 3D graphics support

Multicore Cortex-A53
up to 1.5 GHz
- SIMD engine
- FPU (single, half & double)

ARMv7-R Architecture
up to 600MHz
- RTOS support
- Split-mode or Lock-step
- Tightly coupled memory



Up to 4K UHD (60fps) or 8Kx4K(15fps)
Up to 8 simultaneous streams (full HD)

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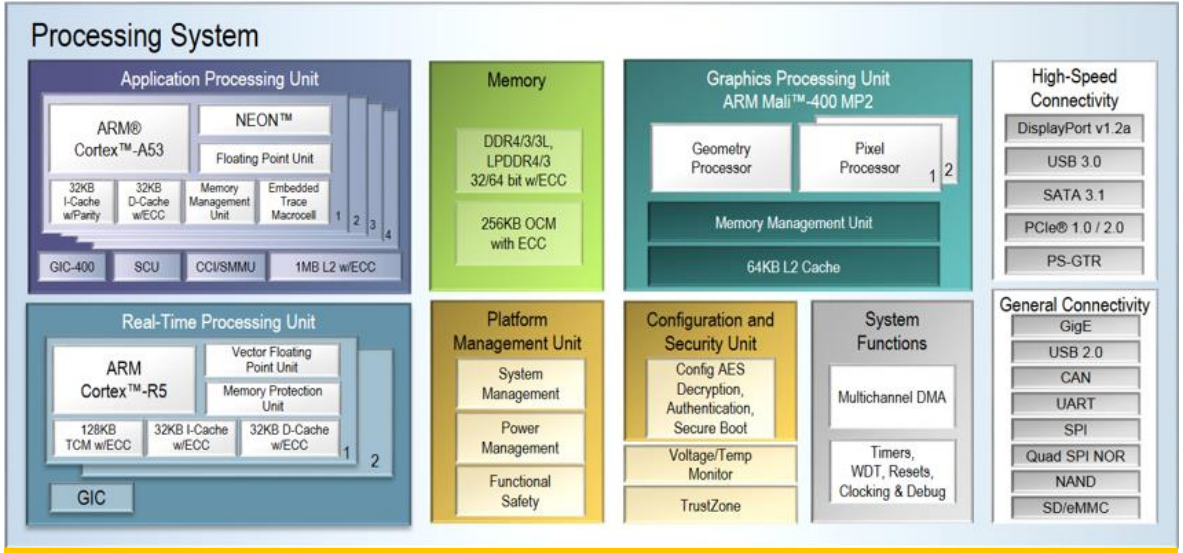
Programmable Logic scalability



XCZU1xx

XCZU7xx

XCZU19EG

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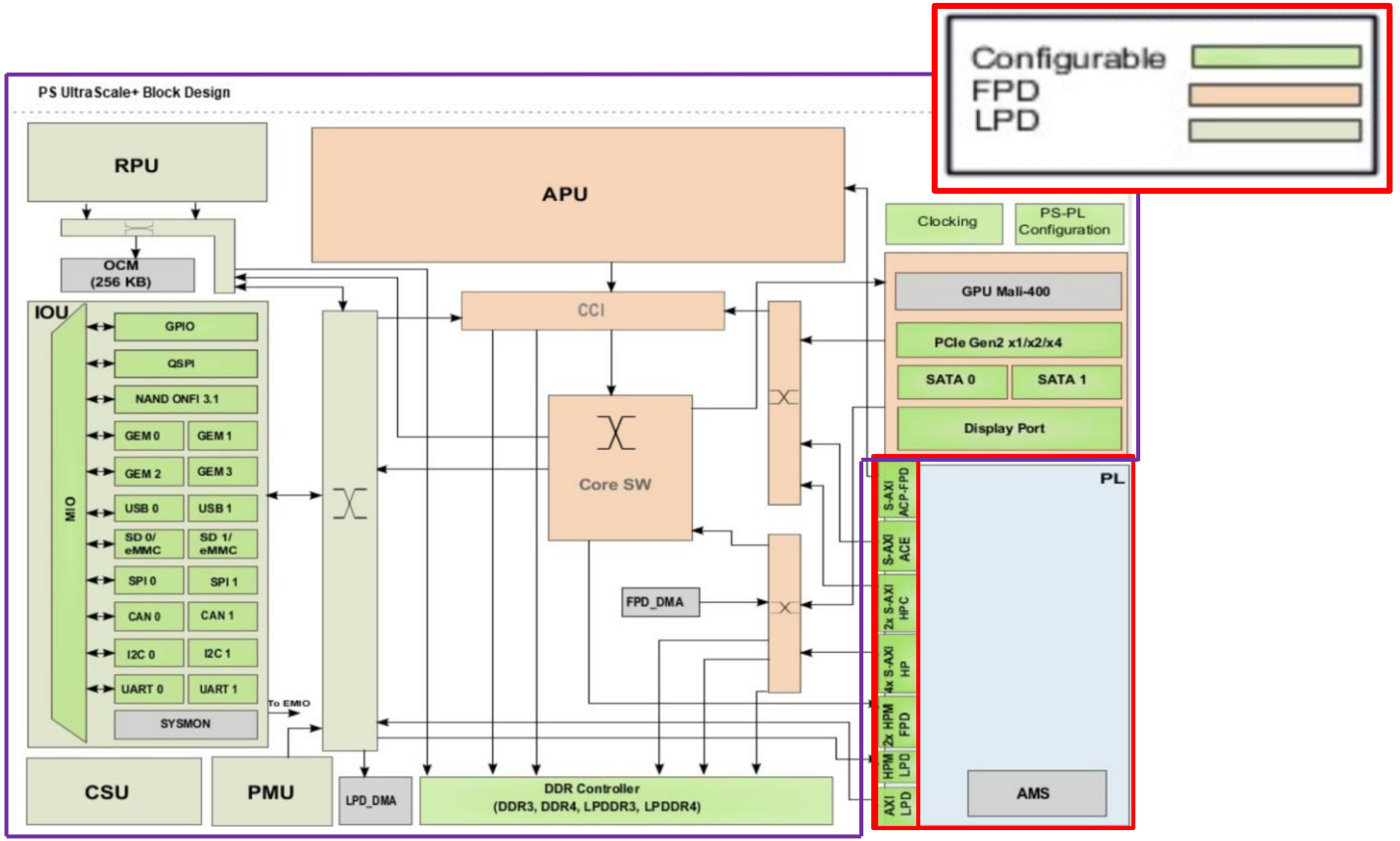
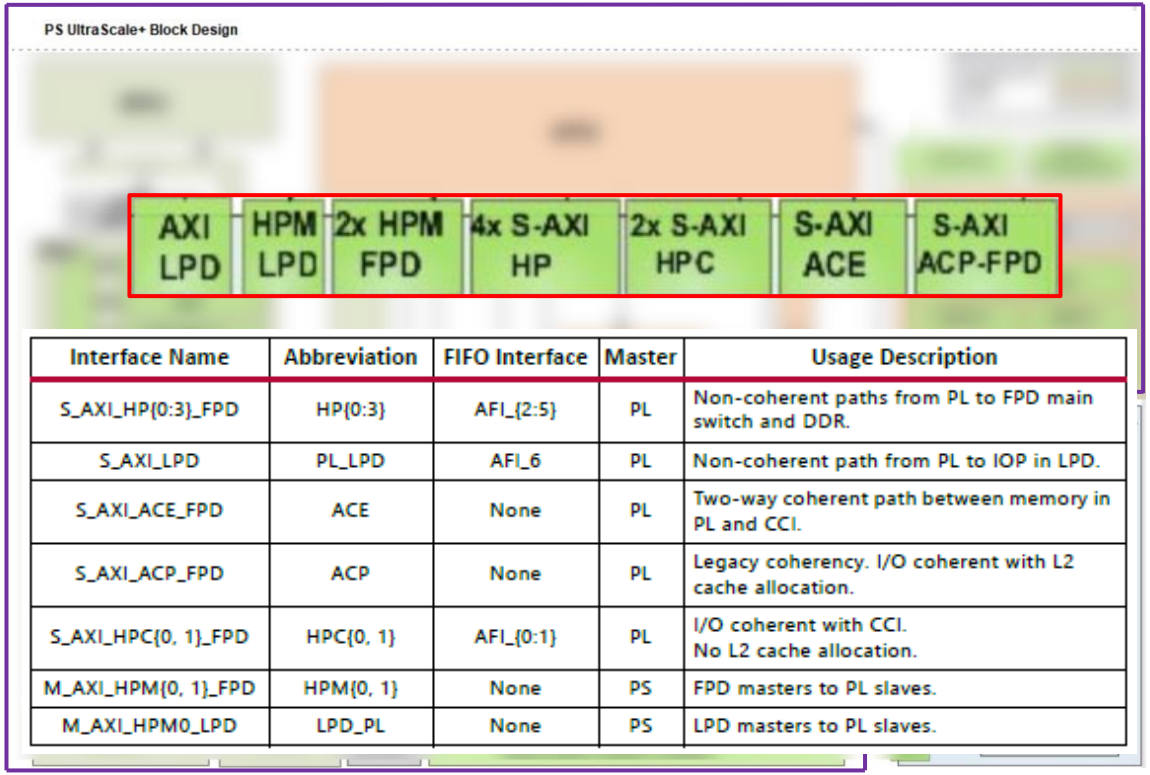
PS-PL Interconnect

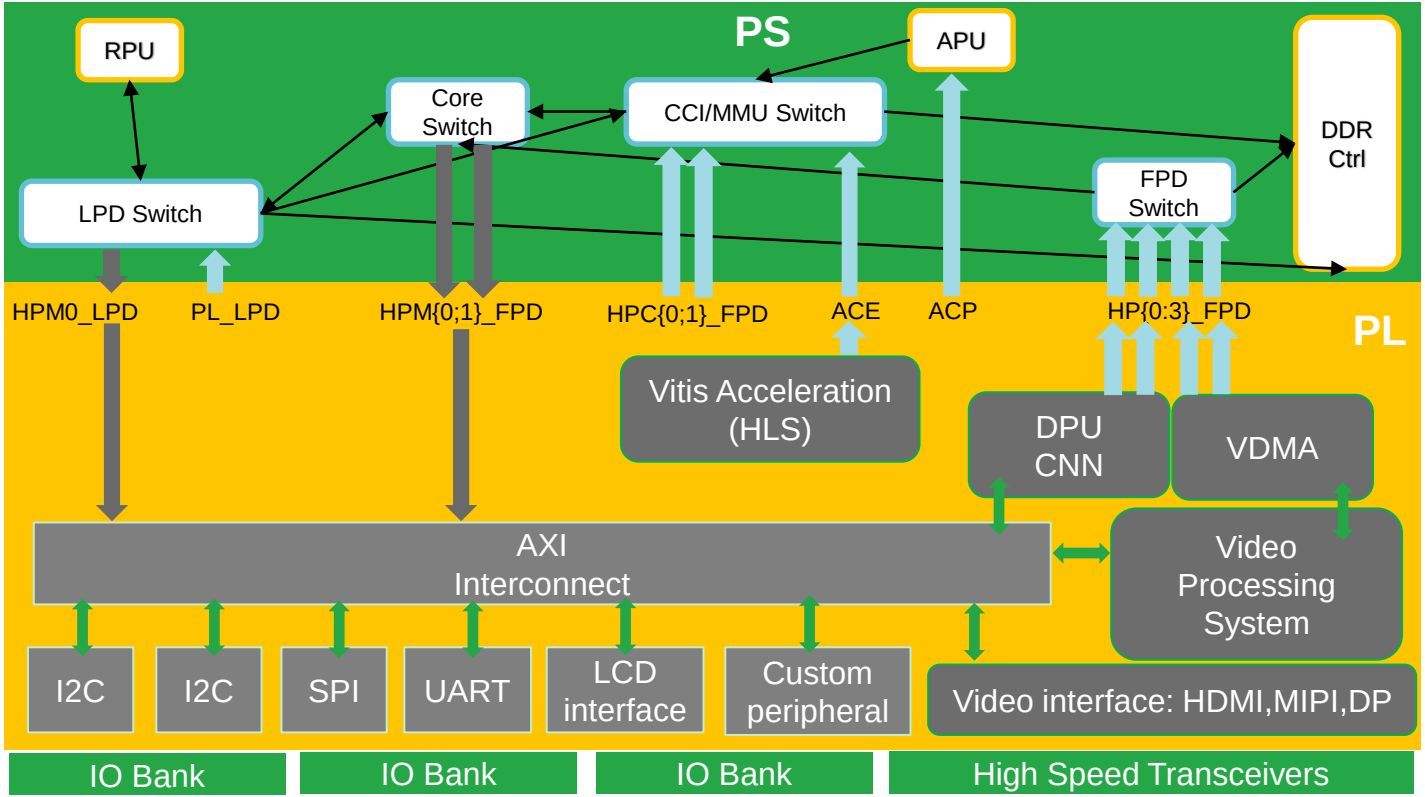


PS-PL Interconnect



Interface Name	Abbreviation	FIFO Interface	Master	Usage Description
S_AXI_HP{0:3}_FPD	HP{0:3}	AFI_{2:5}	PL	Non-coherent paths from PL to FPD main switch and DDR.
S_AXI_LPD	PL_LPD	AFI_6	PL	Non-coherent path from PL to IOP in LPD.
S_AXI_ACE_FPD	ACE	None	PL	Two-way coherent path between memory in PL and CCI.
S_AXI_ACP_FPD	ACP	None	PL	Legacy coherency. I/O coherent with L2 cache allocation.
S_AXI_HPC{0, 1}_FPD	HPC{0, 1}	AFI_{0:1}	PL	I/O coherent with CCI. No L2 cache allocation.
M_AXI_HPM{0, 1}_FPD	HPM{0, 1}	None	PS	FPD masters to PL slaves.
M_AXI_HPM0_LPD	LPD_PL	None	PS	LPD masters to PL slaves.

System Architecture example

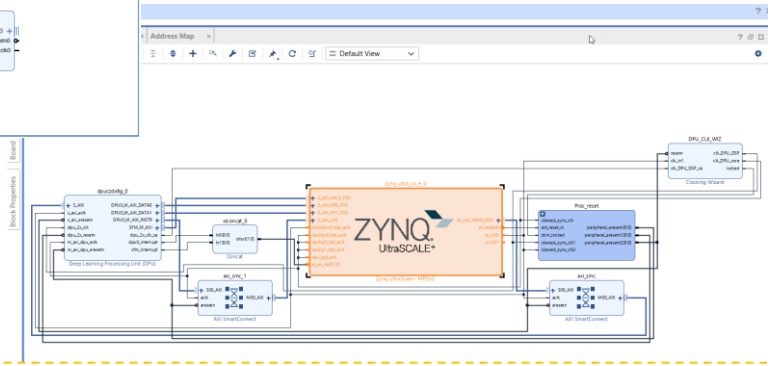


LPDDR4

- Peripheral Extension
- Data Processing (ex: Video)
- Acceleration / CPU offload (ex: Neural Network, HLS)

Zynq Ultrascale+ MPSoC : Development tools

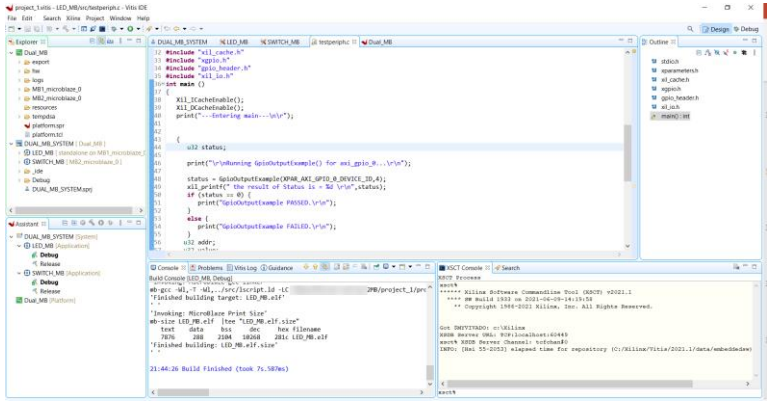
HARDWARE



Export XSA

SOFTWARE

VITIS



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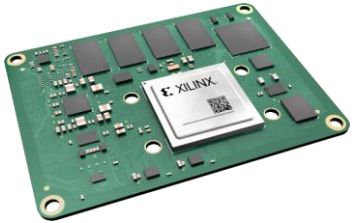
Expanding Our Portfolio with System-on-Modules

Devices	Accelerator Cards	System-On-Modules
		
FPGAs, Adaptive SoCs	x86 Applications	Embedded Applications

A Wide Range of Deployment Methods

Introducing the Xilinx Kria™ System-on-Module Portfolio

KV260
Vision AI Starter Kit

K26
Production SOM Module

DEVELOP ⟶ DEPLOY

Kria KV260 Vision AI Starter Kit

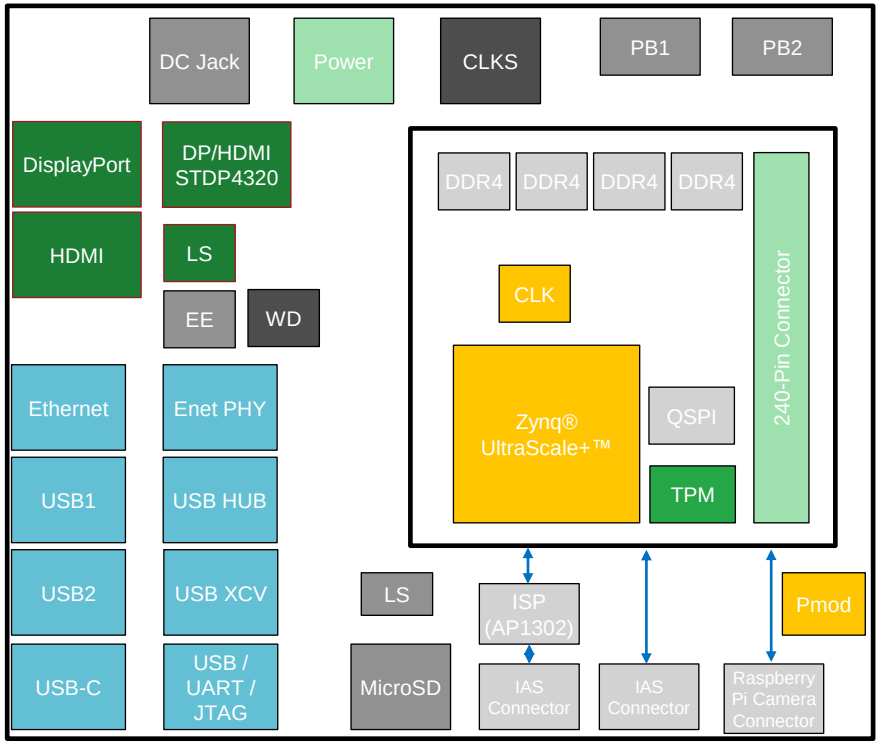
Carrier Card Features & Capabilities

Carrier Card Optimized for Kria SOM
- 240-pin connectivity to SOM
- Targeting vision applications

Vision Ready
- 3 MIPI sensor interfaces, USB cameras
- Built-in ISP component (OnSemi)
- HDMI, DisplayPort outputs

Network & General Connectivity
- 1Gb Ethernet
- USB 3.0 / 2.0

Pmod Expansion
- Extend to any sensor or interface
- Access Pmod ecosystem



119mm x 140mm x 36mm
(SOM + Carrier Card + Heatsink)

Production SOM includes eMMC and additional 240-pin connector

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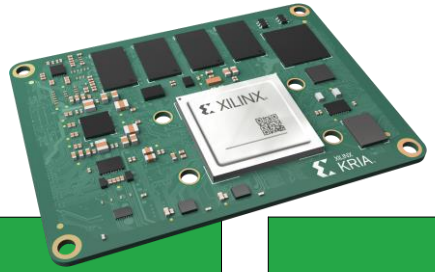
K26 SOM Overview

Based on the Zynq® UltraScale+™ MPSoC Architecture



COMPUTE	
Application Processor	64-bit Quad-Core Arm® Cortex®-A53
Real-Time Processor	32-bit Dual-Core Arm Cortex-R5F
Graphics Processor	Arm Mali™-400MP2
Programmable Logic	256K System Logic Cells
Deep Learning Processor	4K INT8 (upgradable to INT4)
Video Codec (H.264/H.265)	Up to 32 Streams (total resolution ≤ 4Kp60)
Memory	26.6Mb On-Chip SRAM
Security	IEC62443 Security w/HW Root-of-Trust

INTERFACES	
Camera	11 x4 Full MIPI or sub-LVDS Interfaces 1 x4 SLVS-EC Interfaces
USB	4x USB 2.0 / 3.0
Multi-Media	DisplayPort, HDMI
Network	1Gb up to 40Gb Ethernet (w/GigE Vision)
Memory Interface	4GB 64-bit DDR4
Transceivers	4x 12.5Gb/s, 4x 6Gb/s
Mechanical	77 x 60 x 11mm w/ dual 240-pin connectors

Portfolio for Current and Future Market Needs

Performance

ZYNQ RFSoC

Zynq RFSoC Gen 1

4GHz
of Analog Bandwidth

Zynq RFSoC Gen 2

5GHz
of Analog Bandwidth

Zynq RFSoC Gen 3

6GHz
of Analog Bandwidth

IN PRODUCTION

Zynq RFSoC DFE

7.125GHz
of Analog Bandwidth
w/Hardened DFE Subsystem

ASIC Performance with Adaptable Logic

- ✓ More processing per channel
- ✓ Greater instantaneous bandwidth
- ✓ More integration
- ✓ ½ the DC power for a given use case
- ✓ Cost-effective for high volume

2018 2019 2020 2021

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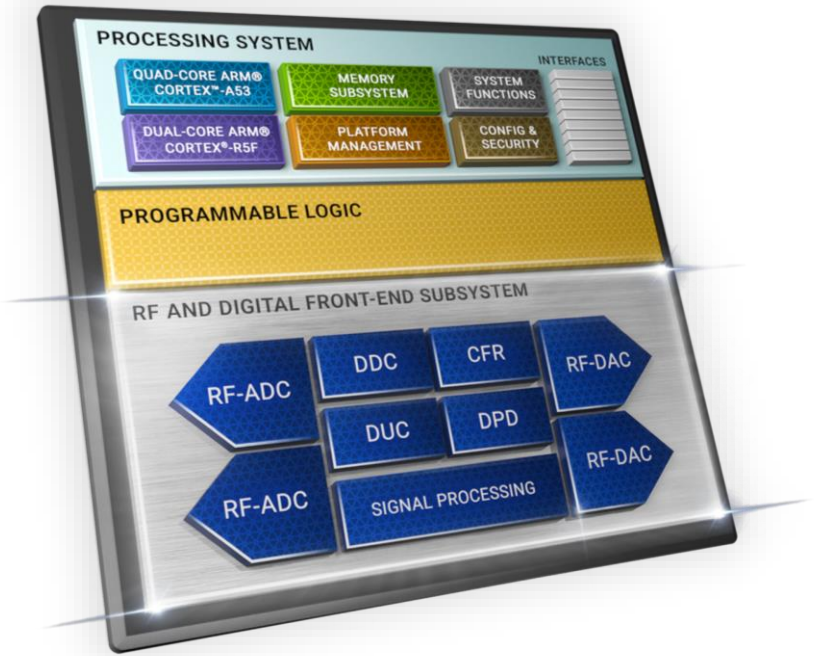
Zynq RFSoC DFE: Adaptive SoC with a Hardened Radio Subsystem



Adaptive SoC

Arm Processing System • UltraScale+ Programmable Logic • 32G SerDes

Hardened Radio Subsystem

Single-Chip 8T8R FDD/TDD

Direct-RF DACs/ADCs
7.125GHz Direct-RF Bandwidth

Digital Pre-Distortion (DPD)
Supports traditional & ultrawide band (400MHz) GaN PAs

Crest Factor Reduction (CFR)
Up to 400MHz of Instantaneous Bandwidth

DUC / DDC[1]
Multi-carrier, multi-band support

Signal Processing IP
FFT/IFFT, PRACH, Re-Sampling, Equalizer

1: Digital Up-Conversion, Digital Down Conversion

Scalability across the Portfolio

		Radio		●	●	●	●	●	●		●	●	●	●	●	●	●	
		Backhaul				●								●				
		Baseband	●															
		Fixed Wireless Access				●	●	●	●		●		●		●	●	●	
		Cable R-PHY				●								●				
		Satellite / Test & Measurement			●		●		●		●	●	●		●	●		
		Radar / SIGINT					●		●		●	●	●		●	●		
			ZU21DR	ZU25DR	ZU27DR	ZU28DR	ZU29DR	ZU39DR	ZU42DR		ZU43DR	ZU46DR		ZU47DR	ZU48DR	ZU49DR	ZU65DR		ZU67DR	
Analog Signal Chain	RF Data Converter Subsystem	RF-ADC w/DDC # of ADCs	-	8	8	8	16	16	8	2	4	8	4	8	8	16	6	8	2
		RF-ADC w/DDC Max ADC rate (GSPS)	-	4.096	4.096	4.096	2.058	2.220	2.5	5.0	5.0	2.5	5.0	5.0	5.0	2.5	5.9	2.95	5.9
		RF-ADC w/DDC Resolution (bits)	-	12	12	12	12	12	14		14	14	14	14	14	14	14	14	
		RF-DAC w/DUC # of DACs	-	8	8	8	16	16	8		4	12		8	8	16	6	6	
		RF-DAC w/DUC Max DAC Rate (GSPS)	-	6.554	6.554	6.554	6.554	6.554	10.0		10.0	10.0		10.0	10.0	10.0	10	10	
		RF-DAC w/DUC Resolution (bits)	-	14	14	14	14	14	14		14	14		14	14	14	14	14	
		SD-FEC	8	-	-	8	-	-	-		-	8		-	8	-	--	--	
		Real multi-band support per ADC	-	1	1	1	1	1	1		2	1		1	1	1			
		RF input Freq max. GHz	4					5	6								7.125		
		Decimation / Interpolation	1x, 2x, 4x, 8x						1x, 2x, 3x, 4x, 5x, 6x, 8x, 10x, 12x, 16x, 20x, 24x, 40x										
Programmable Logic (PL)	Integrated IP	System Logic Cells (K)	930	678	930	930	930	930	488		930	930		930	930	930	489		489	
		DSP Slices	4,272	3,145	4,272	4,272	4,272	4,272	1872		4,272	4,272		4,272	4,272	4,272	1,872		1,872	
		GTY Transceivers	16	8	16	16	16	16	8		16	16		16	16	16	8		8	
		PCIe® Gen 3 x16 / Gen 4 x8	2	1	2	2	2	2	-		2	2		2	2	2	-		-	
		100G Ethernet w/RS-FEC	2	1	2	2	2	2	-		2	2		2	2	2	1		1	
Package Footprint	D1156	35x35																		
	E1156	35x35																		
	G1517	40x40																		
	F1760	42.5x42.5																		
	H1760	42.5x42.5																		

Package Migration

Package Compatible

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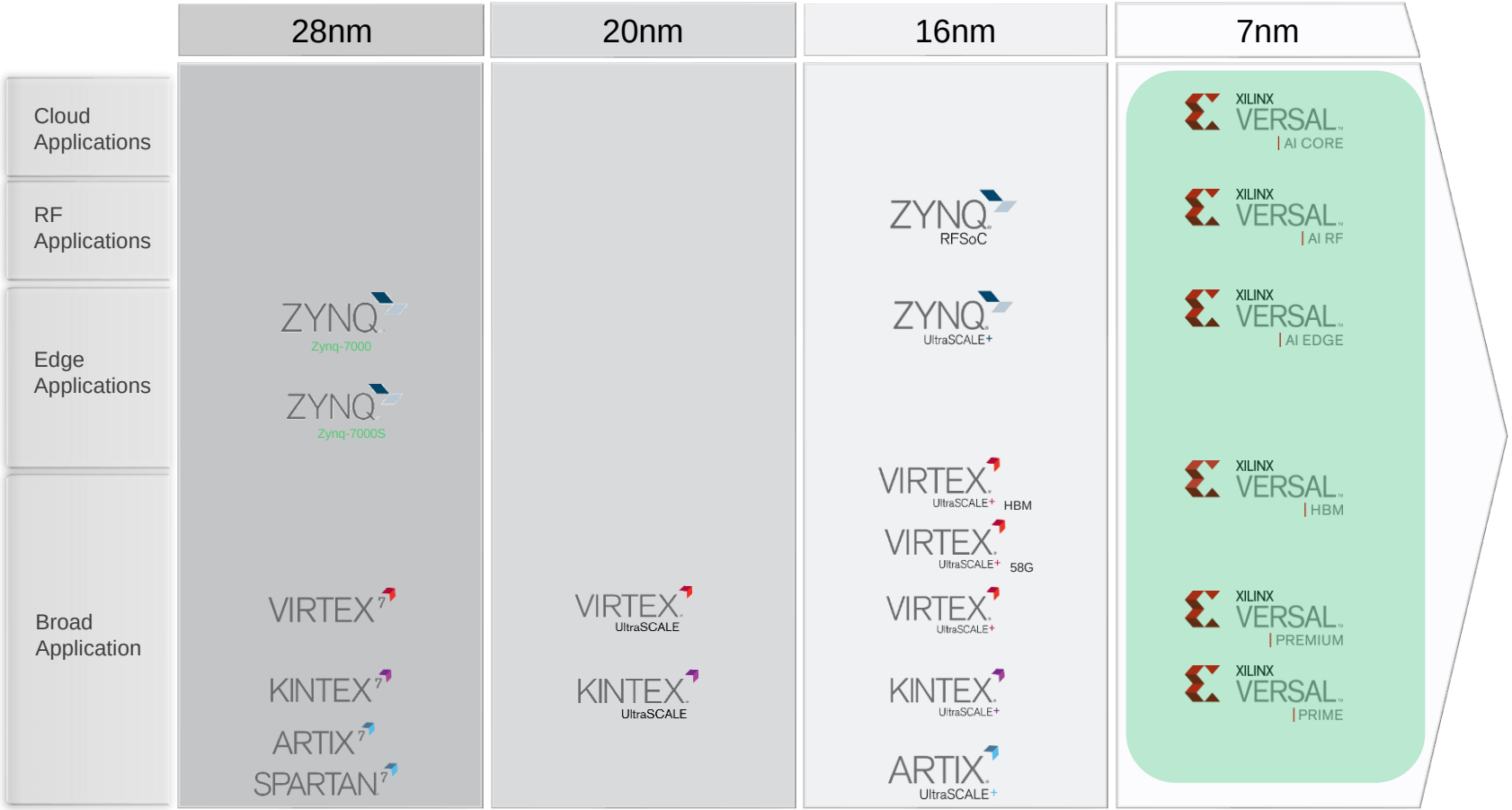
DEMO

Xilinx Portfolio



Versal Architecture Overview

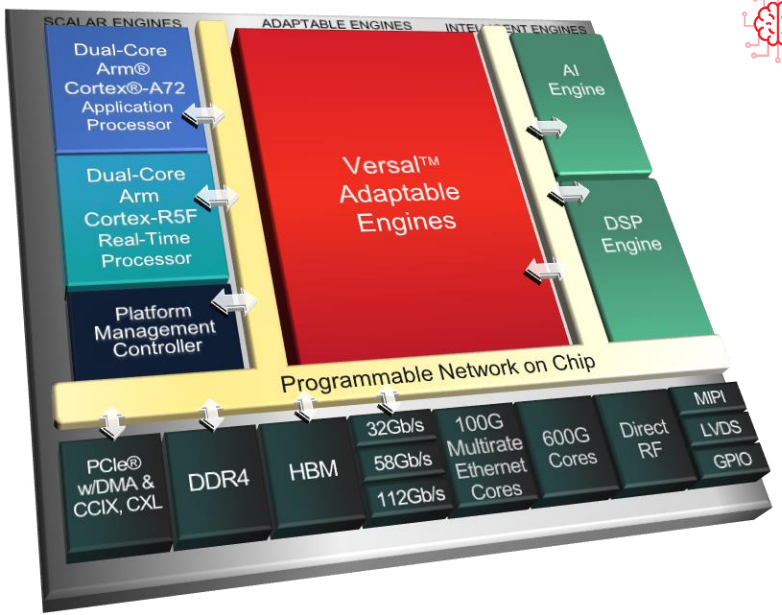
Adaptable Engines
- Re-architected for faster timing closure
- Tune for power vs. performance
- Adaptable to any workload

Scalar Engines
- Platform Control
- Embedded Edge Compute

PCIe Gen5 & CCIX
- 2X PCIe & DMA bandwidth
- Cache-coherency

DDR4 Memory
- 3200-DDR4, 4266-LPDDR4
- 2X bandwidth/pin

Transceiver Leadership
- Broad range, 1G →112G
- 58G in mainstream devices



Intelligent Engines (DSP)
- AI Compute
- Diverse DSP Workloads

Programmable NoC
- Guaranteed Bandwidth
- Enables SW Programmability

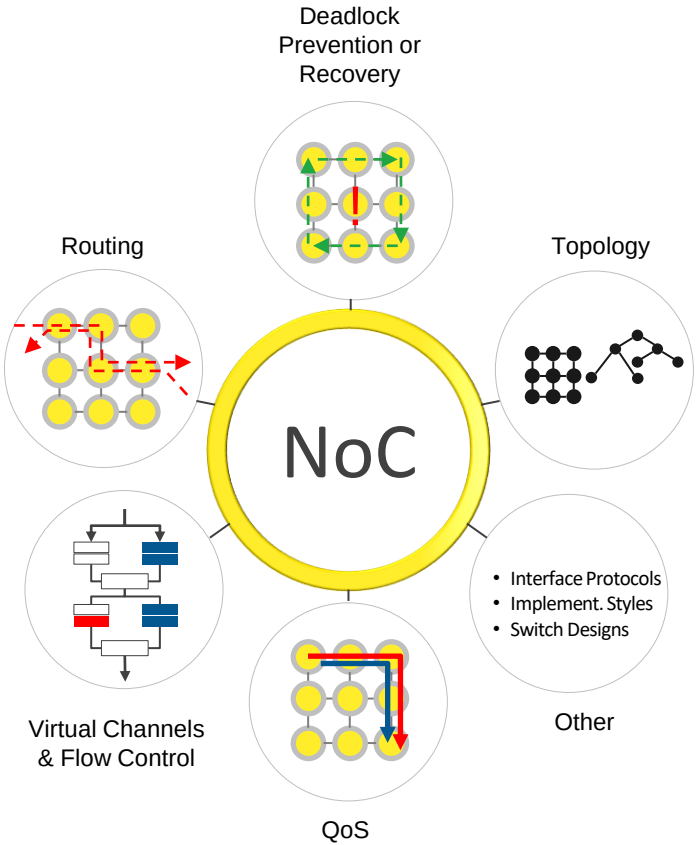
Protocol Engines
- 400G/600G cores
- Power-Optimized

Programmable I/O
- Any interface or sensor
- Includes 3.2Gb/s MIPI

1: 4X logic resources per configurable logic block

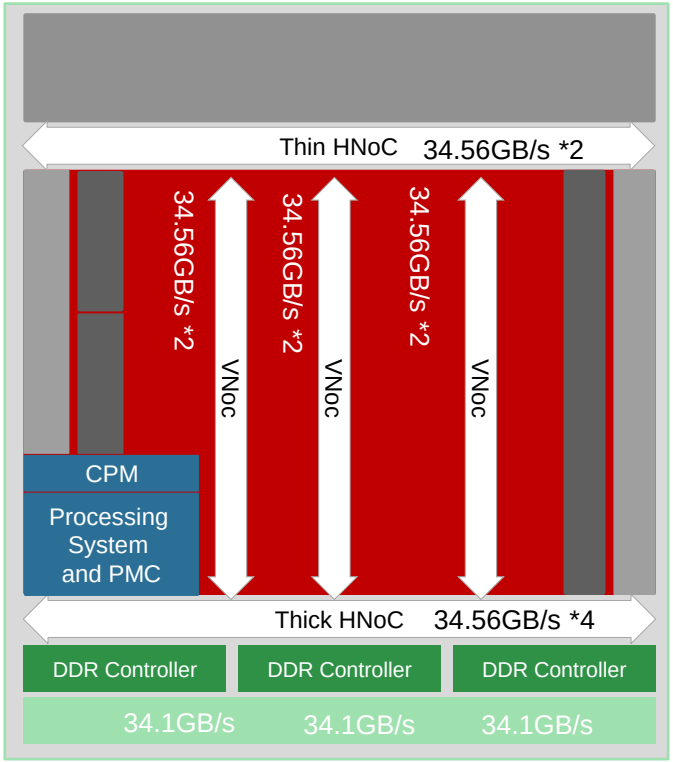
Network on Chip (NoC)

- Device-wide infrastructure component
- High speed (Up to 1080 MHz) hardened data paths
- Facilitates communication between blocks
  - Processing system
  - DDR
  - AI Engines
  - Programmable logic
  - Any other hardened components



NoC and DDRMC Bandwidth Calculations

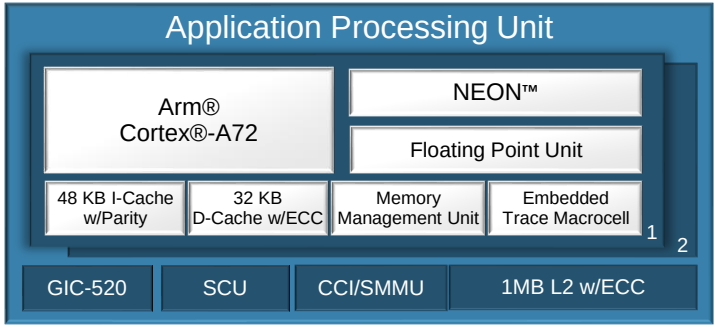
- Each DDRMC will have a maximum bandwidth of 34.1GB/s (LPDDR4 4266)
- Each NoC Lane is independent TX and RX interface (34.56GB/s)
  - TX
    - 1080MHz * 128bits = 138.24Gb/s
    - 138.24/8 =17.28GB/s
  - RX
    - 1080MHz * 128bits = 138.24Gb/s
    - 138.24/8 =17.28GB/s
- Thin Horizontal NoC (HNoC) 2 Lanes
- Vertical NoC (VNoC) 2 Lanes per column this scales with device size
- Thick Horizontal NoC(HNoC) 4 Lanes



The Arm Subsystem

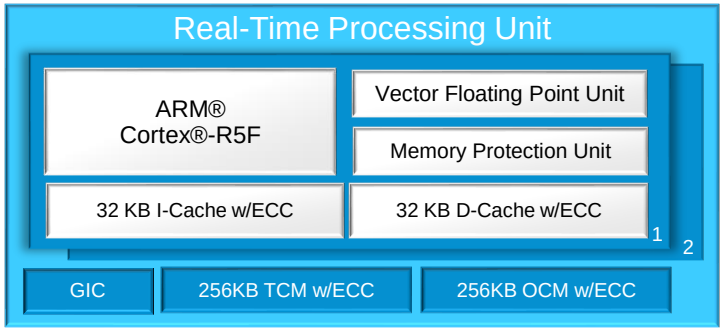
Dual-Core Arm® Cortex®-A72 Application Processor

- Up to 1.7GHz for 2X single-threaded performance[1]
- Power optimized (half the power[1])
- 15.5K – 19.5K DMIPS[2,3] (Dhrystone Benchmark)
- Code portability (Armv8-A architecture)
- Enables SW developers to start from a familiar place



Dual-Core Arm Cortex-R5F Real-Time Processor

- Up to 750MHz for 1.4X greater performance[1]
- Low latency and deterministic
- Flexible operation modes: Split-Mode and Lock-Step
- Highest levels of functional safety (ASIL and SIL)



1: vs. Zynq® UltraScale+™ MPSoCs
2: 15.5K DMIPS at 1.35GHz, -2M Speed Grade, .80V, Dual-Core
3: 19.5K DMIPS at 1.7GHz, -3HP Speed Grade, .88V, Dual-Core

Intelligent Engines
Massive AI Inference Throughput and Wireless Compute

1.3GHz VLIW / SIMD vector processors

- Versatile core for ML and other advanced DSP workloads

Massive array of interconnected cores

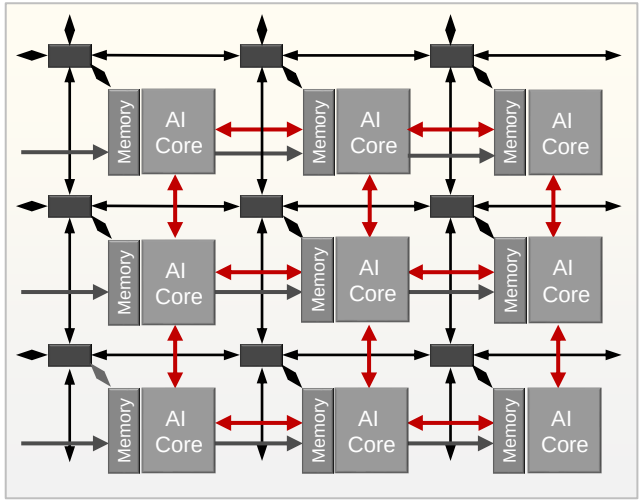
- Instantiate multiple tiles (10s to 100s) for scalable compute

Terabytes/sec of interface bandwidth to other engines

- Direct, massive throughput to adaptable HW engines
- Implement core application with AI for “Whole App Acceleration”

SW programmable for any developer

- C programmable, compile in minutes
- Library-based design for ML framework developers



AI Engine Tile

AI Engine core

- 512b SIMD vector units
  - Both fixed and floating point
  - 16KB program memory
- 32b scalar RISC processor
- 256-bit load/read (x2) and store/write units with individual AGUs

128KB direct core memory access

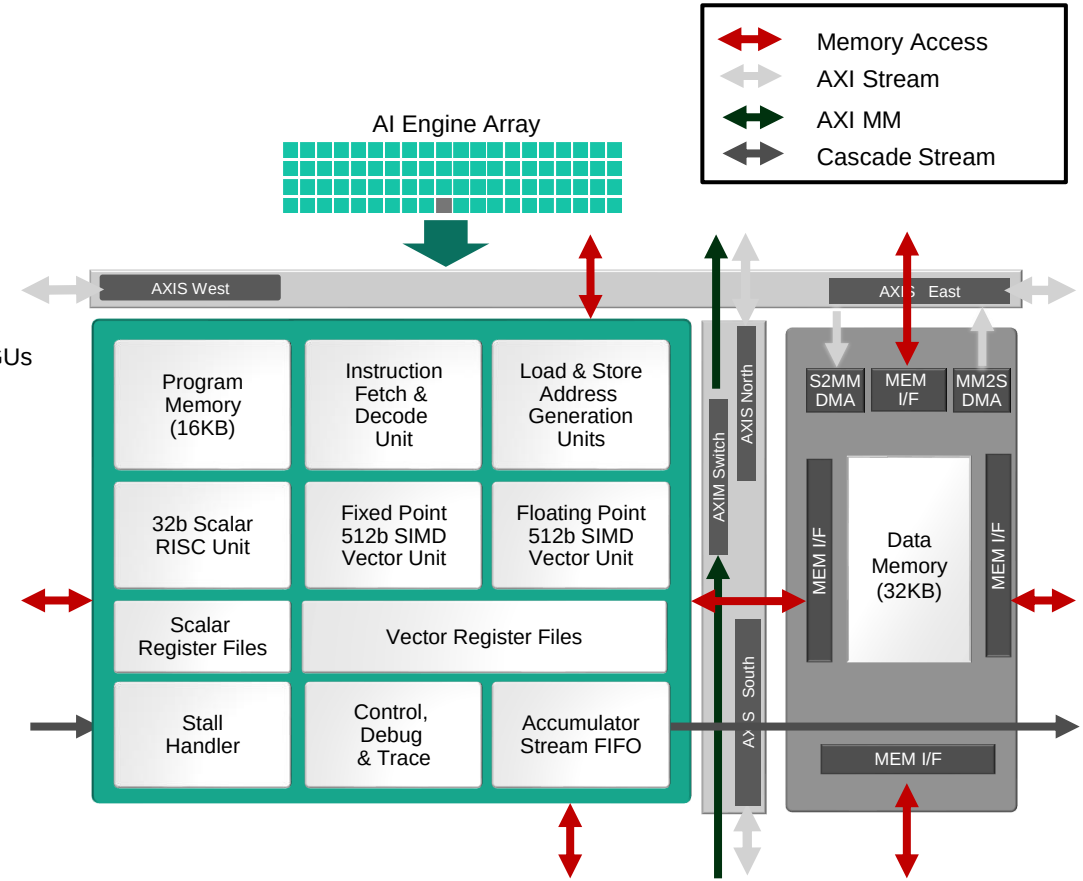
- 32KB local
- 32KB north, south, east or west

Streaming interconnects

- AXI Memory Mapped (AXI-MM) switch
  - Configuration, control and debug
- AXI-Stream crossbar switch
  - Routing N/S/E & W around the array

Debug/Trace/Profile functionality

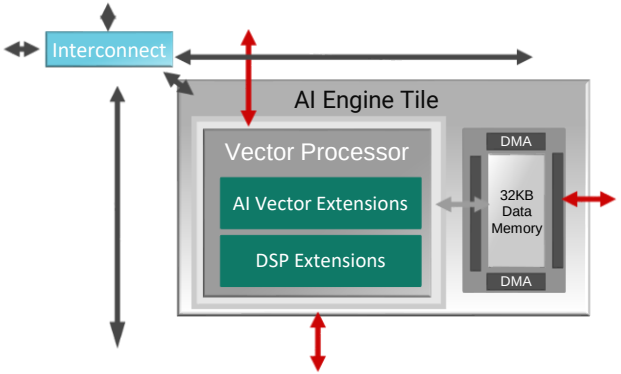
- Debug using memory-mapped AXI4 i/f
- Connect to PMC via JTAG or HSDP



Optimized AI Engine-ML for Up to 4X AI Compute

AI Engine Architecture

Balanced for ML & DSP



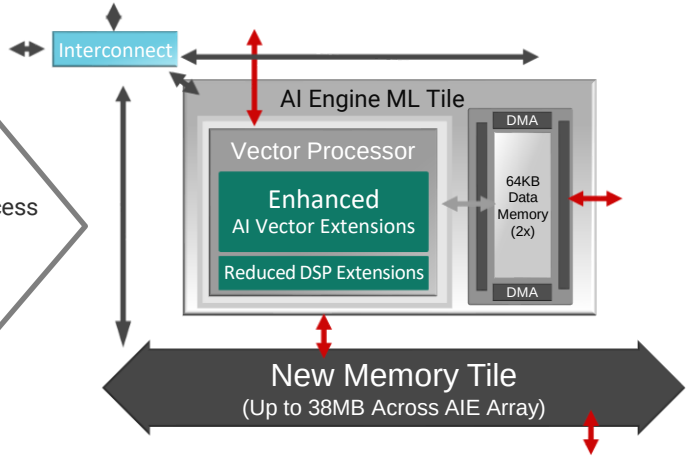
4X ML Compute

at ½ the Latency

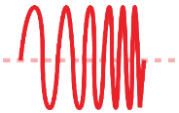
- Enhanced INT8 and added INT4, BFLOAT16
- New MEM Tile for High BW shared mem access
- 2X local data memory per compute core
- Reduced DSP extensions to optimize for ML

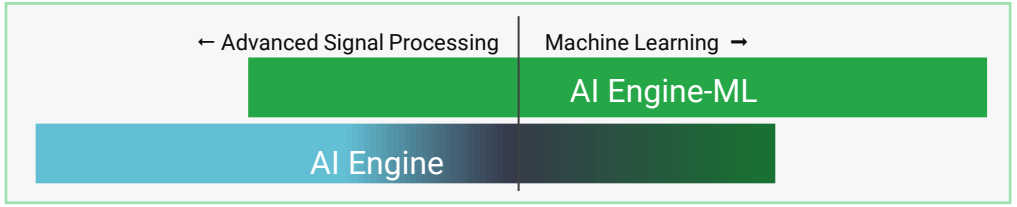
AI Engine-ML Architecture

Optimized for ML



BEAMFORMING,
RADAR PROCESSING,
HIGH PERF. COMPUTING





CNN, RNN, MLP

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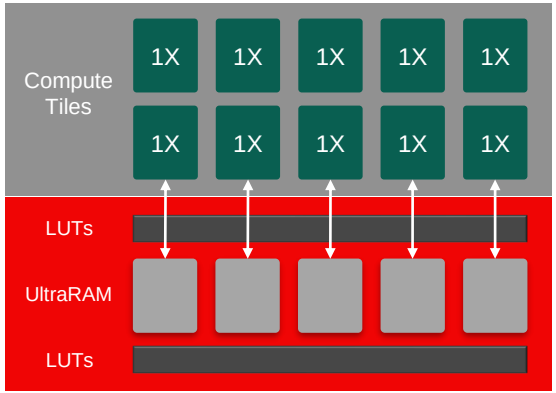
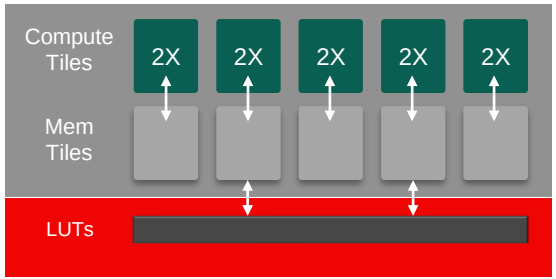
Additional AI Engines-ML Advantages

- Reduced PL footprint due to more local memory in AI Engines-ML
- Fine grained sparsity HW optimization (improves compute by an additional 2X)
- Area per tile increases but fewer tiles per device

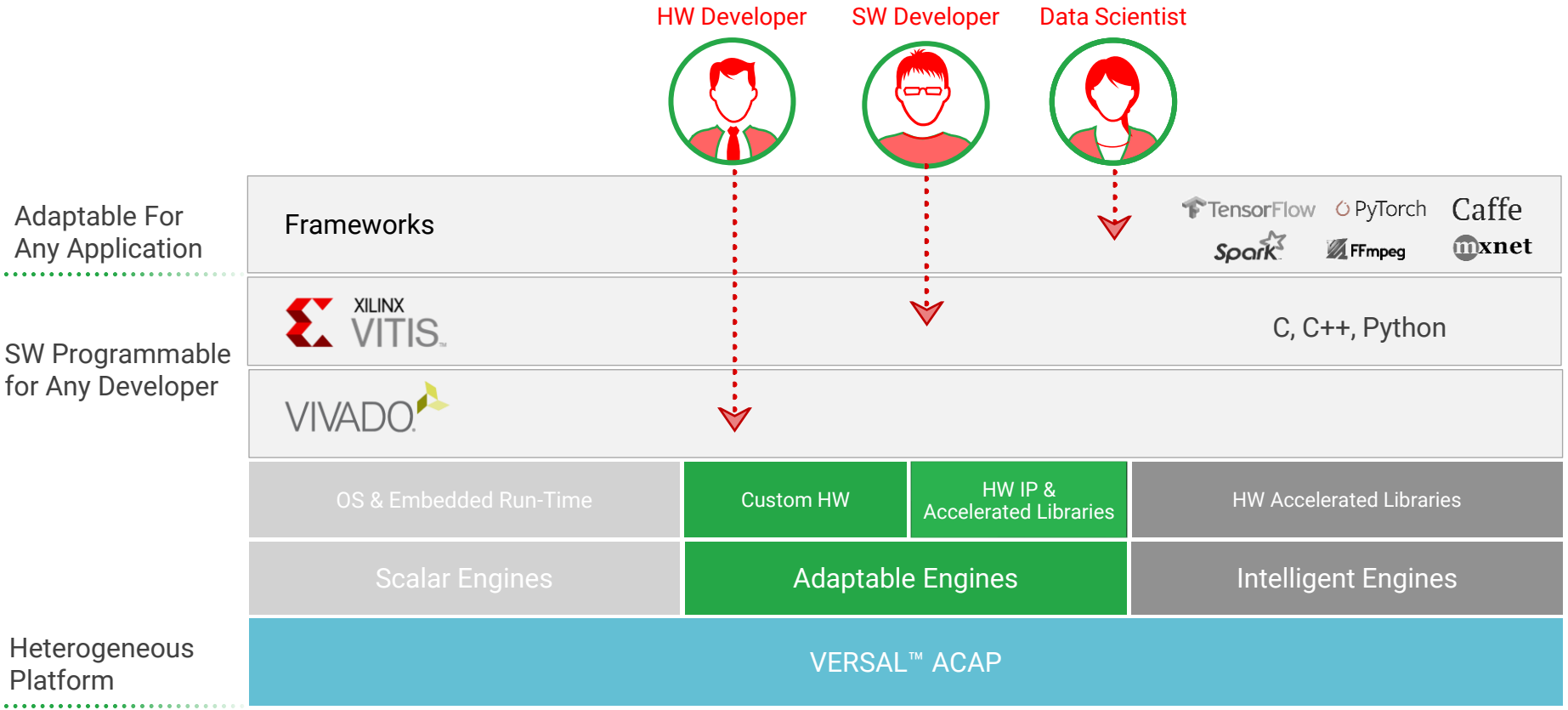
AI Engine Architecture



AIE-ML Architecture



Versal Development Experience for All Developers



Q&A

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AVNET SILICA

ANNEXES

Versal™ ACAPs

AVNET SILICA

Versal® AI Core Series – Resources

		VC1352	VC1502	VC1702	VC1802	VC1902	VC2602	VC2802
Intelligent Engines	AI Engines Tiles	128	198	304	300	400	0	0
	AI Engine-ML Tiles	0	0	0	0	0	152	304
	AI Engine Data Memory (Mb)	32	50	76	75	100	76	152
	AIE-ML Shared Memory (Mb)	0	0	0	0	0	304	304
	DSP Engines	928	1,032	1,312	1,600	1,968	984	1,312
Adaptable Engines	System Logic Cells (K)	540	815	981	1,586	1,968	820	1,139
	LUTs	246,784	372,352	448,512	725,000	899,840	375,000	520,704
	NoC Master / NoC Slave Ports	10	21	21	28	28	21	21
	Distributed RAM (Mb)	8	11	14	22	27	11	16
Memory	Total Block RAM (Mb)	16	30	34	28	34	17	21
	UltraRAM (Mb)	59	110	130	91	130	63	74
	Accelerator RAM (Mb)	32	0	0	0	0	0	0
	Total PL Memory (Mb)	115	151	178	141	191	91	111
	DDR Memory Controllers	2	3	3	4	4	3	3
	DDR Bus Width	128	192	192	256	256	192	192
Scalar Engines	Application Processing Unit	Dual-core Arm® Cortex®-A72, 48KB/32KB L1 Cache w/ parity & ECC; 1MB L2 Cache w/ ECC						
	Real-time Processing Unit	Dual-core Arm Cortex-R5F, 32KB/32KB L1 Cache, and 256KB TCM w/ECC						
	Memory	256KB On-Chip Memory w/ECC						
	Connectivity	Ethernet (x2); UART (x2); CAN-FD (x2); USB 2.0 (x1); SPI (x2); I2C (x2)						
Serial Transceivers	GTY Transceivers (32.75Gb/s)	0	32	44	44	44	0	0
	GTYP Transceivers (32.75Gb/s)	8	0	0	0	0	32(1)	32(1)
Integrated Protocol IP	CCIX & PCIe® w/DMA (CPM)	–	1 x Gen4x16, CCIX	1 x Gen4x16, CCIX	1 x Gen4x16, CCIX	1 x Gen4x16, CCIX	2 x Gen5x8, CCIX	2 x Gen5x8, CCIX
	PCI Express®	1 x Gen4x8	4 x Gen4x8	4 x Gen4x8	4 x Gen4x8	4 x Gen4x8	4 x Gen5x4	4 x Gen5x4
	100G Multirate Ethernet MAC	1	3	4	4	4	2	2
	Video Decoder Engines (VDEs)	–	–	–	–	–	2	4
	Platform Management Controller	Boot, Security, Safety, Monitoring, and High-Speed Debug						
Ordering Information	Extended Temp[2]	-1MSE, -1LSE, -2MSE, -2MLE, -2LSE, -2LLE					-1MSE, -1LSE, -2MSE, -2MLE, -2LSE, -2LLE, -3HSE	
	Industrial Temp[2]	-1MSI, -1MLI, -1LSI, -1LLI, -2MSI, -2MLI, -2LLI, -2HSI					-1MSI, -1MLI, -1LSI, -1LLI, -2MSI, -2MLI	

Notes:

1. 16 GTYP transceivers are dedicated to CPM5 for PCI Express use.
2. In extended and industrial temperature grades, some ordering combinations can operate for a limited time with a junction temperature of 110°C. Timing parameters adhere to the same speed file at 110°C as they do below 110°C, regardless of operating voltage. Operation at 110°C Tj is limited to 3% of the device lifetime and can occur sequentially or at regular intervals as long as the total time does not exceed 3% of device lifetime.

All parameters listed are maximum values. Verify all data in this document with the device data sheets or product guides found at: www.xilinx.com.

Versal® AI Core Series – Packaging

			VC1352	VC1502	VC1702	VC1802	VC1902	VC2602	VC2802
Package	Package Dimensions (mm)	Ball Pitch (mm)	XPIO DDR Only, XPIO DDR+PL HDIO, MIO GTY, GTYP						
NBVA1024	31x31	0.92	168, 210 22, 78 0, 8						
NSVE1369	35x35	0.92	168, 210, 44, 78 0, 8						
NSVG1369	35x35	0.92		132, 246 22, 78 24, 0	132, 246 44, 78 24, 0				
NSVH1369	35x35	0.92						132, 192 44, 78 0, 32	132, 192 44, 78 0, 32
VSVA1596(1)	37.5x37.5	0.92		132, 246 22, 78 32, 0	132, 246 44, 78 32, 0				
VIVA1596(1)	40x40	0.92				132, 246 44, 78 32, 0	132, 246 44, 78 32, 0		
VSVD1760	40x40	0.92				186, 462 0, 78 24, 0	186, 462 0, 78 24, 0		
VFVH1760	40x40	0.92						186, 300 44, 78 0, 32	186, 300 44, 78 0, 32
VSVA2197	45x45	0.92		192, 294 22, 78 32, 0	192, 294 44, 78 44, 0	186, 462 44, 78 44, 0	186, 462 44, 78 44, 0		

All parameters listed are maximum values. Verify all data in this document with the device data sheets or product guides found at: www.xilinx.com.

Versal® AI Edge Series – Resources

		VE2002	VE2102	VE2202	VE2302	VE1752	VE2602	VE2802
Intelligent Engines	AI Engine-ML Tiles	8	12	24	34	0	152	304
	AI Engine Tiles	0	0	0	0	304	0	0
	AIE/AIE-ML Data Memory (Mb)	4	6	12	17	76	76	152
	AIE-ML Shared Memory (Mb)	48	48	68	68	0	304	304
	DSP Engines	90	176	324	464	1,312	984	1,312
Adaptable Engines	System Logic Cells	43,750	80,080	229,688	328,720	981,120	820,313	1,139,040
	LUTs	20,000	36,608	105,000	150,272	448,512	375,000	520,704
	NoC Master / NoC Slave Ports	2	2	5	5	21	21	21
	Distributed RAM (Mb)	0.6	1.1	3.2	4.6	13.7	11.4	15.9
Memory	Total Block RAM (Mb)	0.8	1.7	3.8	5.4	33.5	16.7	21.1
	UltraRAM (Mb)	6.8	13.2	30.4	43.6	129.9	63.0	74.3
	Accelerator RAM (Mb)	32	32	32	32	0	0	0
	Total PL Memory (Mb)	40.2	48	69.4	85.6	177.1	91.1	111.3
	DDR Memory Controllers	1	1	1	1	3	3	3
	DDR Bus Width	64	64	64	64	192	192	192
Scalar Engines	Application Processing Unit	Dual-core Arm® Cortex-A72, 48KB/32KB L1 Cache w/ parity & ECC; 1MB L2 Cache w/ ECC						
	Real-Time Processing Unit	Dual-core Arm Cortex-R5F, 32KB/32KB L1 Cache, and 256KB TCM w/ECC						
	Memory	256KB On-Chip Memory w/ECC						
	Connectivity	Ethernet (x2); UART (x2); CAN-FD (x2); USB 2.0 (x1); SPI (x2); I2C (x2)						
Serial Transceivers	GTY Transceivers	0	0	0	0	44	0	0
	GTYP Transceivers	0	0	8	8	0	32(1)	32(1)
Integrated Protocol IP	CCIX & PCIe® w/DMA (CPM)	-	-	-	-	1 x Gen4x16, CCIX	1 x Gen4x16, CCIX	1 x Gen4x16, CCIX
	PCI Express®	-	-	1 x Gen4x8	1 x Gen4x8	4 x Gen4x8	4 x Gen4x8	4 x Gen4x8
	40G Multirate Ethernet MAC	0	0	1	1	2	2	2
	Video Decoder Engines (VDEs)	–	–	–	–	–	2	4
	Platform Mgmt Controller	Boot, Security, Safety, Monitoring, and High-Speed Debug						
Ordering Information	Extended Temp[2]	-1MSE, -1LSE, -2MSE, -2MLE, -2LSE, -2LLE					-1MSE, -1LSE, -2MSE, -2MLE, -2LSE, -2LLE, -3HSE	
	Industrial Temp[2]	-1MSI, -1MLI, -1LSI, -1LLI, -2MSI, -2MLI, -2LLI, -2HSI					-1MSI, -1MLI, -1LSI, -1LLI, -2MSI, -2MLI	

Notes:

All parameters listed are maximum values. Verify all data in this document with the device data sheets or product guides found at: www.xilinx.com.

1. 16 GTYP transceivers are dedicated to CPM5 for PCI Express use.
2. In extended and industrial temperature grades, some ordering combinations can operate for a limited time with a junction temperature of 110°C. Timing parameters adhere to the same speed file at 110°C as they do below 110°C, regardless of operating voltage. Operation at 110°C Tj is limited to 3% of the device lifetime and can occur sequentially or at regular intervals as long as the total time does not exceed 3% of device lifetime.

Versal® AI Edge Series – Packaging

			VE2002	VE2102	VE2202	VE2302	VE1752	VE2602	VE2802
Package Footprint	Package Dimensions (mm)	Ball Pitch (mm)	XPIO DDR Only, XPIO DDR+PL HDIO, MIO GTY, GTYP						
SBVA484	19x19	0.8	84, 30 0, 78 0, 0	84, 30 0, 78 0, 0					
SBVA625	21x21	0.8	132, 84 0, 78 0, 0	132, 84 0, 78 0, 0					
SFVA784	23x23	0.8	132, 84 0, 78 0, 0	132, 84 0, 78 0, 0	132, 84 22, 78 0, 8	132, 84 22, 78 0, 8			
NSVG1369	35x35	0.92					132, 246 44, 78 24, 0		
NSVH1369	35x35	0.92						132, 192 44, 78 0, 32	132, 192 44, 78 0, 32
VSVA1596[(1)]	37.5x37.5	0.92					132, 246 44, 78 32, 0		
VFVH1760	40x40	0.92						186, 300 44, 78 0, 32	186, 300 44, 78 0, 32
VSVA2197	45x45	0.92					192, 294 44, 78 44, 0		

Notes:
1. VE1752 in the VSVA1596 package supports peak LPDDR4 data rates in 324 I/O only. The remaining 54 I/O support limited data rates. See the associated data sheet.

All parameters listed are maximum values. Verify all data in this document with the device data sheets or product guides found at: www.xilinx.com.

Versal® Prime Series – Resources

		VM1102	VM1302	VM1402	VM1502	VM1802	VM2202	VM2302	VM2502	VM2902
Adaptable Engines	System Logic Cells (K)	329	693	1,238	981	1,968	1,139	1,575	1,969	2,233
	LUTs	150,272	316,928	565,760	448,512	899,840	520,704	719,872	900,224	1,020,928
	NoC Master / NoC Slave Ports	5	9	18	21	28	21	30	28	42
	Distributed RAM (Mb)	5	10	17	14	27	16	22	27	31
Memory	Total Block RAM (Mb)	5	18	40	34	34	21	49	47	70
	Total UltraRAM (Mb)	44	50	80	130	130	74	127	190	181
	Total PL Memory (Mb)	54	78	137	178	191	111	198	264	282
	DDR Memory Controllers	1	2	4	3	4	3	3	4	3
	DDR Bus Widths	64	128	256	192	256	192	192	256	192
Intelligent Engines	DSP Engines	464	832	1,696	1,312	1,968	1,312	1,904	3,984	2,672
Scalar Engines	Application Processing Unit	Dual-core Arm® Cortex-A72, 48KB/32KB L1 Cache w/ parity & ECC; 1MB L2 Cache w/ ECC								
	Real-time Processing Unit	Dual-core Arm Cortex-R5F, 32KB/32KB L1 Cache, and 256KB TCM w/ECC								
	Memory	256KB On-Chip Memory w/ECC								
	Connectivity	Ethernet (x2); USB 2.0 (x1); UART (x2); SPI (x2); I2C (x2); CAN-FD (x2)								
Serial Transceivers	GTY Transceivers	0	24	24	44	44	0	0	0	0
	GTYP Transceivers	8	0	0	0	0	32(1)	8	28(1)	8
	GTM Transceivers (56Gb/s)	0	0	0	0	0	0	40	20	40
Integrated Protocol IP	CCIX & PCIe® w/DMA (CPM)	-	1 x Gen4x16, CCIX	1 x Gen4x16, CCIX	1 x Gen4x16, CCIX	1 x Gen4x16, CCIX	2 x Gen5x8, CCIX	-	2 x Gen5x8, CCIX	-
	PCI Express®	1 x Gen4x8	2 x Gen4x8	2 x Gen4x8	4 x Gen4x8	4 x Gen4x8	4 x Gen5x4	2 x Gen5x4	2 x Gen5x4	2 x Gen5x4
	100G Multirate Ethernet MAC	1	2	2	4	4	2	6	2	6
Ordering Information	Extended Temp[2]	-1MSE, -1LSE, -2MSE, -2MLE, -2LSE, -2LLE					-1MSE, -1LSE, -2MSE, -2MLE, -2LSE, -2LLE, -3HSE			
	Industrial Temp[2]	-1MSI, -1MLI, -1LSI, -1LLI, -2MSI, -2MLI, -2LLI, -2HSI					-1MSI, -1MLI, -1LSI, -1LLI, -2MSI, -2MLI			

Notes:
1. 16 GTYP transceivers are dedicated to the CPM for PCI Express use.
2. In extended and industrial temperature grades, some ordering combinations can operate for a limited time with a junction temperature of 110°C. Timing parameters adhere to the same speed file at 110°C as they do below 110°C, regardless of operating voltage. Operation at 110°C Tj is limited to 3% of the device lifetime and can occur sequentially or at regular intervals as long as the total time does not exceed 3% of device lifetime.

All parameters listed are maximum values. Verify all data in this document with the device data sheets or product guides found at: www.xilinx.com.

Versal® Prime Series – Packaging

			VM1102	VM1302	VM1402	VM1502	VM1802	VM2202	VM2302	VM2502	VM2902
Package	Package Dimensions (mm)	Ball Pitch (mm)	XPIO DDR Only, XPIO DDR+PL HDIO, MIO GTY, GTYP, GTM								
SFVA784	23x23	0.8	132, 84 22, 78 0, 8, 0								
NBVB1024	31x31	0.92		132, 84 22, 78 16, 0, 0	132, 192 22, 78 16, 0, 0						
NFVB1369	35x35	0.92				132, 246 22, 78 16, 0, 0					
NSVF1369	35x35	0.92		168, 156 22, 78 8, 0, 0	168, 480 22, 78 8, 0, 0						
VFVC1596	37.5x37.5	0.92		168, 264 22, 78 24, 0, 0	168, 480 22, 78 24, 0, 0						
VFVC1760[1]	40x40	0.92				132, 246 44, 78 44, 0, 0	132, 246 44, 78 44, 0, 0				
VSVD1760[2,3]	40x40	0.92		168, 156 0, 78 16, 0, 0	168, 480 0, 78 16, 0, 0		186, 462 0, 78 24, 0, 0				
VFVF1760[4]	40x40	0.92							180, 306 22, 78 0, 8, 40		180, 306 22, 78 0, 8, 40
VSVA2197	45x45	0.92				192, 294 44, 78 44, 0, 0	186, 462 44, 78 44, 0, 0				
VSVC2197[4]	45x45	0.92						186, 300 44, 78 0, 32, 0		132, 516 0, 78 0, 28, 20	

1. Devices in VFVC1760 support peak LPDDR4 in 162 I/O only. The remaining 216 I/O support limited data rates. See the associated data sheet.
2. VM1302 in VSVD1760 supports peak LPDDR4 in 162 I/O only. The remaining 162 I/O support limited data rates. See the associated data sheet.
3. VM1402 in VSVD1760 supports peak LPDDR4 in 324 I/O only. The remaining 324 I/O support limited data rates. See the associated data sheet.
4. Some packages are compatible with Versal Premium series devices.

Versal® Premium Series – Resources

		VP1002	VP1052	VP1102	VP1202	VP1402	VP1502	VP2502	VP1552	VP1702	VP1802	VP2802
Adaptable Engines	System Logic Cells (K)	833	1,186	1,575	1,969	2,233	3,763	3,738	3,837	5,558	7,352	7,326
	LUTs	380,800	542,080	719,872	900,224	1,020,928	1,720,448	1,708,672	1,753,984	2,540,672	3,360,896	3,349,120
	NoC Master / NoC Slave Ports	22	22	30	28	42	52	52	52	76	100	100
	Distributed RAM (Mb)	12	17	22	27	31	53	52	54	78	103	102
Memory	Total Block RAM (Mb)	19	26	49	47	70	89	89	89	132	174	174
	UltraRAM (Mb)	97	138	127	190	181	366	366	366	541	717	717
	Total PL Memory (Mb)	128	181	198	264	282	508	507	509	751	994	994
	DDR Memory Controllers	2	2	3	4	3	4	4	4	4	4	4
	DDR Bus Width	128	128	192	256	192	256	256	256	256	256	256
Intelligent Engines	DSP Engines	1,140	1,572	1,904	3,984	2,672	7,440	7,392	7,392	10,896	14,352	14,304
	AI Engines Tiles	-	-	-	-	-	-	472	-	-	-	472
	AI Engine Data Memory (Mb)	-	-	-	-	-	-	118	-	-	-	118
Scalar Engines	APU	Dual-core Arm® Cortex®-A72, 48KB/32KB L1 Cache w/ parity & ECC; 1MB L2 Cache w/ ECC										
	RPU	Dual-core Arm Cortex-R5F, 32KB/32KB L1 Cache, and 256KB TCM w/ECC										
	Memory	256KB On-Chip Memory w/ECC										
	Connectivity	Ethernet (x2); UART (x2); CAN-FD (x2); USB 2.0 (x1); SPI (x2); I2C (x2)										
Serial Transceivers	GTY Transceivers (32.75Gb/s)	20	20	-	-	-	-	-	-	-	-	-
	GTYP Transceivers (32.75Gb/s)	-	-	8	28(1)	8	28(1)	28(1)	68(1)	28(1)	28(1)	28(1)
	GTM Transceivers(2) (58G (112G))	24 (12)	48 (24)	64 (32)	20 (10)	96 (64)	60 (30)	60 (30)	20 (10)	100 (50)	140 (70)	140 (70)
Integrated Protocol IP	PCIe® w/DMA & CCIX (CPM4)	2 x Gen4x4	2 x Gen4x4	-	-	-	-	-	-	-	-	-
	PCIe w/DMA & CCIX (CPM5)	-	-	-	2 x Gen5x8	-	2 x Gen5x8	2 x Gen5x8	2 x Gen5x8	2 x Gen5x8	2 x Gen5x8	2 x Gen5x8
	PCI Express	1 x Gen4x8	1 x Gen4x8	2 x Gen5x4	2 x Gen5x4	2 x Gen5x4	2 x Gen5x4	2 x Gen5x4	8 x Gen5x4	2 x Gen5x4	2 x Gen5x4	2 x Gen5x4
	100G Multirate Ethernet MAC	3	5	6	2	6	4	4	4	6	8	8
	600G Ethernet MAC	2	3	7	1	11	3	3	1	5	7	7
	600G Interlaken	1	2	0	0	0	1	1	0	2	3	3
	400G High-Speed Crypto Engine	1	1	3	1	4	2	2	2	3	4	4
Ordering Information	Extended(3)	-1MSE, -1LSE, -2MSE, -2MLE, -2LSE, -2LLE		-1MSE, -1LSE, -2MSE, -2MLE, -2LSE, -2LLE, -3HSE								
	Industrial(3)	-1MSI, -1MLI, -1LSI, -1LLI, -2MSI, -2MLI, -2LLI, -2HSI		-1MSI, -1MLI, -1LSI, -1LLI, -2MSI, -2MLI								

Notes:
1. 16 GTYP transceivers are dedicated to the CPM5 for PCI Express use.
2. GTM transceivers can operate at data rates up to 112Gb/s by combining two transceivers together. The VP1402 device in the VSVD2197 package can run 64 GTM transceivers at 112Gb/s.
3. In extended and industrial temperature grades, some ordering combinations can operate for a limited time with a junction temperature of 110°C. Timing parameters adhere to the same speed file at 110°C as they do below 110°C regardless of operating voltage. Operation at 110°C Tj is limited to 3% of the device lifetime and can occur sequentially or at regular intervals as long as the total time does not exceed 3% of device lifetime.

All parameters listed are maximum values. Verify all data in this document with the device data sheets or product guides found at: www.xilinx.com.

Versal® Premium Series – Packaging

			VP1002	VP1052	VP1102	VP1202	VP1402	VP1502	VP2502	VP1552	VP1702	VP1802	VP2802
Package	Package Dimensions (mm)	Ball Pitch (mm)	XPIO DDR Only, XPIO DDR+PL HDIO, MIO GTY, GTM (112G)		XPIO DDR Only, XPIO DDR+PL HDIO, MIO GTYP, GTM (112G)								
NFVI1369	35x35	0.92	138, 24 0, 78 8, 24 (12)	138, 24 0, 78 8, 36 (18)									
VFVF1760[1]	40x40	0.92	192, 132 0, 78 8, 24 (12)	192, 132 0, 78 8, 36 (18)	132, 192 22, 78 8, 40 (20)		132, 192 22, 78 8, 40 (20)						
VSVC2021	45x45	0.92	192, 186 0, 78 20, 24 (12)	192, 186 0, 78 20, 48 (24)									
VSVC2197[1]	45x45	0.92				132, 516 0, 78 28, 20 (10)							
VSVD2197	45x45	0.92					0, 54 0, 78 8, 96 (64)[3]						
VSVA2785[2]	50x50	0.92			180, 306 44, 78 8, 64 (32)	132, 570 0, 78 28, 20 (10)	180, 306 44, 78 8, 80 (40)	132, 570 0, 78 28, 56 (28)		132, 570 0, 78 68, 16 (8)			
VSVA3340	55x55	0.92					180, 306 44, 78 8, 96 (48)	132, 354 0, 78 28, 60 (30)		132, 354 0, 78 68, 20 (10)	132, 354 0, 78 28, 88 (44)		
VSVB3340	55x55	0.92							132, 570 0, 78 28, 60 (30)				
LSVC4072	65x65	1.0										132, 570 0, 78 28, 140 (70)	
VSVA5601	70x70	0.92							132, 570 0, 78 28, 60 (30)		132, 570 0, 78 28, 100 (50)	132, 570 0, 78 28, 140 (70)	132, 570 0, 78 28, 140 (70)

2. VP1202, VP1502, and VP1552 in VSVA2785 support peak LPDDR4 data rates in 486 I/O only. The remaining 216 I/O support limited data rates. See the associated data sheet.
3. GTM transceivers can operate at data rates up to 112Gb/s by combining two transceivers together. The VP1402 device in the VSVD2197 package can run 64 GTM transceivers at 112Gb/s.

Versal® HBM Series – Resources & Packaging

		VH1522	VH1542	VH1582	VH1742	VH1782
Adaptable Engines	System Logic Cells (K)	3,837	3,837	3,837	5,631	5,631
	LUTs	1,753,984	1,753,984	1,753,984	2,574,208	2,574,208
	NoC Master / NoC Slave Ports	52	52	52	76	76
	Distributed RAM (Mb)	54	54	54	79	79
Memory	Total Block RAM (Mb)	89	89	89	132	132
	UltraRAM (Mb)	366	366	366	541	541
	Total PL Memory (Mb)	509	509	509	752	752
	HBM DRAM (GB)	8	16	32	16	32
	DDR Memory Controllers	4	4	4	4	4
	DDR Bus Width	256	256	256	256	256
Intelligent Engines	DSP Engines	7,392	7,392	7,392	10,848	10,848
Scalar Engines	APU	Dual-core Arm® Cortex-A72, 48KB/32KB L1 Cache w/ parity & ECC; 1MB L2 Cache w/ ECC				
	RPU	Dual-core Arm Cortex-R5F, 32KB/32KB L1 Cache, and 256KB TCM w/ECC				
	Memory	256KB On-Chip Memory w/ECC				
	Connectivity	Ethernet (x2); UART (x2); CAN-FD (x2); USB 2.0 (x1); SPI (x2); I2C (x2)				
Serial Transceivers	GTYP Transceivers (32.75Gb/s)	68(1)	68(1)	68(1)	68(1)	68(1)
	GTM Transceivers(2) (56G (112G))	20 (10)	20 (10)	20 (10)	60 (30)	60 (30)
Integrated Protocol IP	CCIX & PCIe® w/DMA (CPM5)	2 x Gen5x8, CCIX	2 x Gen5x8, CCIX	2 x Gen5x8, CCIX	2 x Gen5x8, CCIX	2 x Gen5x8, CCIX
	PCI Express (PLPCIE5)	8 x Gen5x4	8 x Gen5x4	8 x Gen5x4	8 x Gen5x4	8 x Gen5x4
	100G Multirate Ethernet MAC	4	4	4	6	6
	600G Ethernet MAC	1	1	1	3	3
	600G Interlaken	0	0	0	1	1
	400G High-Speed Crypto Engines	2	2	2	3	3
Ordering Information	Extended Temp	-1MSE, -1LSE, -2MSE, -2MLE, -2LSE, -2LLE, -3HSE				
	Industrial Temp	–				

Package Footprint	Package Dimensions (mm)	Ball Pitch (mm)	XPIO DDR Only, XPIO DDR+PL HDIO, MIO GTYP, GTM (112G)				
VSVA3697	57.5x57.5	0.92	132, 570 0, 78 68, 20 (10)	132, 570 0, 78 68, 20 (10)	132, 570 0, 78 68, 20 (10)		
LSVA4737	70x70	1.0		132, 570 0, 78 68, 20 (10)	132, 570 0, 78 68, 20 (10)	132, 570 0, 78 68, 60 (30)	132, 570 0, 78 68, 60 (30)

Notes:
1. 16 GTYP transceivers are dedicated to CPM5 for PCI Express use.
2. GTM transceivers can operate at data rates up to 112Gb/s by combining two transceivers together.

UltraScale+™ Devices

Zynq® UltraScale+™ RFSoCs – Resources

	Device Name	ZU21DR	ZU25DR	ZU27DR	ZU28DR	ZU29DR	ZU39DR	ZU42DR	ZU43DR	ZU46DR	ZU47DR	ZU48DR	ZU49DR	ZU65DR	ZU67DR
		Gen 1					Gen 2	Gen 3						DFE	
PS		**Quad-core** Arm® Cortex®-A53 MPCore™ up to 1.3GHz, **Dual-core** Arm Cortex-R5F MPCore up to 533MHz													
RF Data Converter	12-bit RF-ADC w/DDC # of ADCs	0	8	8	8	16	16	–	–	–	–	–	–	–	–
	12-bit RF-ADC w/DDC Max Rate (GSPS)	0	4.096	4.096	4.096	2.058	2.220	–	–	–	–	–	–	–	–
	14-bit RF-ADC w/DDC # of ADCs	–	–	–	–	–	–	8 2	4	8 4	8	8	16	6	8 2
	14-bit RF-ADC w/DDC Max Rate (GSPS)	–	–	–	–	–	–	2.5 5.0	5.0	2.5 5.0	5.0	5.0	2.5	5.9	2.95 5.9
	14-bit RF-DAC w/DUC # of DACs	0	8	8	8	16	16	8	4	12	8	8	16	6	8
	14-bit RF-DAC w/DUC Max Rate (GSPS)	0	6.554	6.554	6.554	6.554	6.554	9.85[3]	9.85[3]	9.85[3]	9.85[3]	9.85[3]	9.85[3]	10.0[4]	10.0[4]
	SD-FEC	8	0	0	8	0	0	0	0	8	0	8	0	0	0
	Digital Front-End (DFE)	–	–	–	–	–	–	–	–	–	–	–	–	✓	✓
	Number of DDCs per RF-ADC[1]	0	1	1	1	1	1	1	2	1	1	1	1	1	1
	RF input Freq max. GHz			4			5			6				7.125	
	Decimation / Interpolation	1x, 2x, 4x, 8x					1x, 2x, 4x, 8x	1x, 2x, 3x, 4x, 5x, 6x, 8x, 10x, 12x, 16x, 20x, 24x, 40x						1x, 2x, 3x, 4x, 5x, 6x, 8x, 10x, 12x, 16x, 20x, 24x, 40x	
Programmable Logic (PL)	System Logic Cells (K)	930	678	930	930	930	930	489	930	930	930	930	930	489	489
	CLB LUTs (K)	425	310	425	425	425	425	224	425	425	425	425	425	224	224
	Max. Dist. RAM (Mb)	13.0	9.6	13.0	13.0	13.0	13.0	6.8	13.0	13.0	13.0	13.0	13.0	6.8	6.8
	Total Block RAM (Mb)	38.0	27.8	38.0	38.0	38.0	38.0	22.8	38.0	38.0	38.0	38.0	38.0	22.8	22.8
	UltraRAM (Mb)	22.5	13.5	22.5	22.5	22.5	22.5	45.0	22.5	22.5	22.5	22.5	22.5	45.0	45.0
	DSP Slices	4,272	3,145	4,272	4,272	4,272	4,272	1,872	4,272	4,272	4,272	4,272	4,272	1,872	1,872
	GTY Transceivers	16	8	16	16	16	16	8	16	16	16	16	16	8	8
	PCIe® Gen3 x16	2	1	2	2	2	2	–	–	–	–	–	–	–	–
	PCIeGen3 x16/Gen4 x8 / CCIX[2]	–	–	–	–	–	–	0	2	2	2	2	2	0	0
	150G Interlaken	1	1	1	1	1	1	0	1	1	1	1	1	0	0
	100G Ethernet MAC/PCS w/RS-FEC	2	1	2	2	2	2	0	2	2	2	2	2	1	1
	System Monitor	2	2	2	2	2	2	2	2	2 2	2	2	2	2	2
	Speed Grades	-1E, -1I, -1LI, -2E, -2LE, -2I, -2LI	-1E, -1I, -1LI, -2E, -2LE, -2I, -2LI	-1E, -1I, -1LI, -2E, -2LE, -2I, -2LI	-1E, -1I, -1LI, -2E, -2LE, -2I, -2LI	-1E, -1I, -1LI, -2E, -2LE, -2I, -2LI	-2I, -2LI	-1E, -1I, -1LI, -2E, -2I, -2LI	-1E, -1I, -1LI, -2E, -2I, -2LI	-1E, -1I, -1LI, -2E, -2I, -2LI	-1E, -1I, -1LI, -2E, -2I, -2LI	-1E, -1I, -1LI, -2E, -2I, -2LI	-1E, -1I, -1LI, -2E, -2I, -2LI	-1I, -1LI, -2I, -2LI	-1I, -1LI, -2I, -2LI

Notes
1. This value applies when all RF I/O of an RF-ADC tile are used.
2. This block operates in compatibility mode for 16.0GT/s (Gen4) operation. See PG213.
3. For operation up to 10GSPS, contact your local Xilinx Sales Representative.
4. 4. 10GSPS RF-DAC operation is available in -2I speed grade.

Product Tables

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Zynq® UltraScale+™ RFSoCs – Packaging

	Device Name	ZU21DR	ZU25DR	ZU27DR	ZU28DR	ZU29DR	ZU39DR	ZU42DR	ZU43DR	ZU46DR	ZU47DR	ZU48DR	ZU49DR	ZU65DR	ZU67DR
		Gen 1					Gen 2	Gen 3						DFE	
Package Footprint	Package Dimensions	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC
D1156	35x35	214, 72, 208 4, 16 0, 0													
E1156	35x35		214, 48, 104 4, 8 8, 8	214, 48, 104 4, 8 8, 8	214, 48, 104 4, 8 8, 8			214, 24, 128 4, 8 10, 8	214, 48, 104 4, 8 4, 4		214, 48, 104 4, 8 8, 8	214, 48, 104 4, 8 8, 8		214, 24, 130 4, 8 6, 6	214, 24, 130 4, 8 10, 8
G1517	40x40		214, 48, 299 4, 8 8, 8	214, 48, 299 4, 16 8, 8	214, 48, 299 4, 16 8, 8				214, 48, 299 4, 16 4, 4		214, 48, 299 4, 16 8, 8	214, 48, 299 4, 16 8, 8			
F1760	42.5x42.5					214, 96, 312 4, 16 16, 16	214, 96, 312 4, 16 16, 16						214, 96, 312 4, 16 16, 16		
H1760	42.5x42.5									214, 48, 312 4, 16 12, 12					

Zynq® UltraScale+™ MPSoCs: CG Devices

		Device Name[1]	ZU1CG	ZU2CG	ZU3CG	ZU4CG	ZU5CG	ZU6CG	ZU7CG	ZU9CG
Processing System (PS)	Application Processor Unit	Processor Core	**Dual-core** Arm® Cortex®-A53 MPCore™ up to 1.3GHz							
		Memory w/ECC	L1 Cache 32KB I / D per core, L2 Cache 1MB, on-chip Memory 256KB							
	Real-Time Processor Unit	Processor Core	**Dual-core** Arm Cortex-R5F MPCore up to 533MHz							
		Memory w/ECC	L1 Cache 32KB I / D per core, Tightly Coupled Memory 128KB per core							
	External Memory	Dynamic Memory Interface	x16: DDR4 w/o ECC; x32/x64: DDR4, LPDDR4, DDR3, DDR3L, LPDDR3 w/ ECC							
		Static Memory Interfaces	NAND, 2x Quad-SPI							
	Connectivity	High-Speed Connectivity	PCIe® Gen2 x4, 2x USB3.0, SATA 3.1, DisplayPort, 4x Tri-mode Gigabit Ethernet							
		General Connectivity	2xUSB 2.0, 2x SD/SDIO, 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO							
	Integrated Block Functionality	Power Management	Full / Low / PL / Battery Power Domains							
		Security	RSA, AES, and SHA							
		AMS - System Monitor	10-bit, 1MSPS – Temperature and Voltage Monitor							
PS to PL Interface			12 x 32/64/128b AXI Ports							
Programmable Logic (PL)	Programmable Functionality	System Logic Cells (K)	81	103	154	192	256	469	504	600
		CLB Flip-Flops (K)	74	94	141	176	234	429	461	548
		CLB LUTs (K)	37	47	71	88	117	215	230	274
	Memory	Max. Distributed RAM (Mb)	1.0	1.2	1.8	2.6	3.5	6.9	6.2	8.8
		Total Block RAM (Mb)	3.8	5.3	7.6	4.5	5.1	25.1	11.0	32.1
		UltraRAM (Mb)	-	-	-	13.5	18.0	-	27.0	-
	Clocking	Clock Management Tiles (CMTs)	3	3	3	4	4	4	8	4
	Integrated IP	DSP Slices	216	240	360	728	1,248	1,973	1,728	2,520
		PCI Express® Gen 3x16	-	-	-	2	2	-	2	-
		150G Interlaken	-	-	-	-	-	-	-	-
		100G Ethernet MAC/PCS w/RS-FEC	-	-	-	-	-	-	-	-
		AMS - System Monitor	1	1	1	1	1	1	1	1
	Transceivers	GTH 16.3Gb/s Transceivers	-	-	-	16	16	24	24	24
		GTY 32.75Gb/s Transceivers	-	-	-	-	-	-	-	-
	Speed Grades	Extended[2]	-1 -2 -2L							
		Industrial	-1 -1L -2							

Notes:
1. For full part number details, see the Ordering Information section in DS891, *Zynq UltraScale+ MPSoC Overview*.
2.-2LE (Tj = 0°C to 110°C). For more details, see the Ordering Information section in DS891, *Zynq UltraScale+ MPSoC Overview*.

Zynq® UltraScale+™ MPSoCs: EG Devices

		Device Name[1]	ZU1EG	ZU2EG	ZU3EG	ZU4EG	ZU5EG	ZU6EG	ZU7EG	ZU9EG	ZU11EG	ZU15EG	ZU17EG	ZU19EG
Processing System (PS)	Application Processor Unit	Processor Core	**Quad-core** Arm® Cortex®-A53 MPCore™ up to 1.5GHz											
		Memory w/ECC	L1 Cache 32KB I / D per core, L2 Cache 1MB, on-chip Memory 256KB											
	Real-Time Processor Unit	Processor Core	**Dual-core** Arm Cortex-R5F MPCore™ up to 600MHz											
		Memory w/ECC	L1 Cache 32KB I / D per core, Tightly Coupled Memory 128KB per core											
	Graphic & Video Acceleration	Graphics Processing Unit	Mali™-400 MP2 up to 667MHz											
		Memory	L2 Cache 64KB											
	External Memory	Dynamic Memory Interface	x16: DDR4 w/o ECC; x32/x64: DDR4, LPDDR4, DDR3, DDR3L, LPDDR3 w/ ECC											
		Static Memory Interfaces	NAND, 2x Quad-SPI											
	Connectivity	High-Speed Connectivity	PCIe® Gen2 x4, 2x USB3.0, SATA 3.1, DisplayPort, 4x Tri-mode Gigabit Ethernet											
		General Connectivity	2xUSB 2.0, 2x SD/SDIO, 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO											
	Integrated Block Functionality	Power Management	Full / Low / PL / Battery Power Domains											
		Security	RSA, AES, and SHA											
		AMS - System Monitor	10-bit, 1MSPS – Temperature and Voltage Monitor											
PS to PL Interface			12 x 32/64/128b AXI Ports											
Programmable Logic (PL)	Programmable Functionality	System Logic Cells (K)	81	103	154	192	256	469	504	600	653	747	926	1,143
		CLB Flip-Flops (K)	74	94	141	176	234	429	461	548	597	682	847	1,045
		CLB LUTs (K)	37	47	71	88	117	215	230	274	299	341	423	523
	Memory	Max. Distributed RAM (Mb)	1.0	1.2	1.8	2.6	3.5	6.9	6.2	8.8	9.1	11.3	8.0	9.8
		Total Block RAM (Mb)	3.8	5.3	7.6	4.5	5.1	25.1	11.0	32.1	21.1	26.2	28.0	34.6
		UltraRAM (Mb)	-	-	-	13.5	18.0	-	27.0	-	22.5	31.5	28.7	36.0
	Clocking	Clock Management Tiles (CMTs)	3	3	3	4	4	4	8	4	8	4	11	11
	Integrated IP	DSP Slices	216	240	360	728	1,248	1,973	1,728	2,520	2,928	3,528	1,590	1,968
		PCI Express® Gen 3x16	-	-	-	2	2	-	2	-	4	-	4	5
		150G Interlaken	-	-	-	-	-	-	-	-	1	-	2	4
		100G Ethernet MAC/PCS w/RS-FEC	-	-	-	-	-	-	-	-	2	-	2	4
		AMS - System Monitor	1	1	1	1	1	1	1	1	1	1	1	1
	Transceivers	GTH 16.3Gb/s Transceivers	-	-	-	16	16	24	24	24	32	24	44	44
		GTY 32.75Gb/s Transceivers	-	-	-	-	-	-	-	-	16	-	28	28
	Speed Grades	Extended[2]	-1 -2 -2L			-1 -2 -2L -3					-1 -2 -2L -3			
		Industrial	-1 -1L -2											

Notes:
1. For full part number details, see the Ordering Information section in DS891, *Zynq UltraScale+ MPSoC Overview*.
2.-2LE (Tj = 0°C to 110°C). For more details, see the Ordering Information section in DS891, *Zynq UltraScale+ MPSoC Overview*.

Zynq® UltraScale+™ MPSoCs: CG / EG Devices

Pkg Footprint[2,3]	Dimensions (mm)	Ball Pitch (mm)	ZU1	ZU2	ZU3	ZU4	ZU5	ZU6	ZU7	ZU9	ZU11	ZU15	ZU17	ZU19
A484[4]	19x19	0.8	170, 24, 58 4, 0, 0	170, 24, 58 4, 0, 0	170, 24, 58 4, 0, 0									
A494	9.5x15	0.5	170, 24, 58 4, 0, 0											
A530	9.5x16	0.5		170, 24, 58 4, 0, 0	170, 24, 58 4, 0, 0									
A625[4]	21x21	0.8	170, 24, 156 4, 0, 0	170, 24, 156 4, 0, 0	170, 24, 156 4, 0, 0									
C784[4,5]	23x23	0.8	214, 24, 156, 4, 0, 0	214, 96, 156 4, 0, 0	214, 96, 156 4, 0, 0	214, 96, 156 4, 4, 0	214, 96, 156 4, 4, 0							
B900	31x31	1.0				214, 48, 156 4, 16, 0	214, 48, 156 4, 16, 0		214, 48, 156 4, 16, 0					
C900	31x31	1.0						214, 48, 156 4, 16, 0		214, 48, 156 4, 16, 0		214, 48, 156 4, 16, 0		
B1156	35x35	1.0						214, 120, 208 4, 24, 0		214, 120, 208 4, 24, 0		214, 120, 208 4, 24, 0		
C1156	35x35	1.0							214, 48, 312 4, 20, 0		214, 48, 312 4, 20, 0			
B1517	40x40	1.0									214, 72, 416 4, 16, 0		214, 72, 572 4, 16, 0	214, 72, 572 4, 16, 0
F1517	40x40	1.0							214, 48, 416 4, 24, 0		214, 48, 416 4, 32, 0			
C1760	42.5x42.5	1.0									214, 96, 416 4, 32, 16		214, 96, 416 4, 32, 16	214, 96, 416 4, 32, 16
D1760	42.5x42.5	1.0											214, 48, 260 4, 44, 28	214, 48, 260 4, 44, 28
E1924	45x45	1.0											214, 96, 572 4, 44, 0	214, 96, 572 4, 44, 0

Notes:
1. PS I/O is a combination of PS MIO and PS DDRIO.
2. Packages with the same last letter and number sequence, e.g., A484, are footprint compatible with all other UltraScale devices with the same sequence.
3. For full part number details, see the Ordering Information section in DS891, *Zynq UltraScale+ MPSoC Overview*.
4. These packages are only offered in 0.8mm ballpitch. All other packages are offered in 1.0mm ball pitch.
5. GTH transceivers in the C784 package support data rates up to 12.5Gb/s.

Virtex® UltraScale+™ FPGAs

		Foundation							58G PAM4		
	Device Name	VU3P	VU5P	VU7P	VU9P	VU11P	VU13P	VU19P	VU23P	VU27P	VU29P
	System Logic Cells (K)	862	1,314	1,724	2,586	2,835	3,780	8,938	2,252	2,835	3,780
	CLB Flip-Flops (K)	788	1,201	1,576	2,364	2,592	3,456	8,172	2,059	2,592	3,456
	CLB LUTs (K)	394	601	788	1,182	1,296	1,728	4,086	1,030	1,296	1,728
	Max. Dist. RAM (Mb)	12.0	18.3	24.1	36.1	36.2	48.3	58.4	14.2	36.2	48.3
	Total Block RAM (Mb)	25.3	36.0	50.6	75.9	70.9	94.5	75.9	74.3	70.9	94.5
	UltraRAM (Mb)	90.0	132.2	180.0	270.0	270.0	360.0	90.0	99.0	270.0	360.0
	DSP Slices	2,280	3,474	4,560	6,840	9,216	12,288	3,840	1,320	9,216	12,288
	Peak INT8 DSP (TOP/s)	7.1	10.8	14.2	21.3	28.7	38.3	10.4	4.1	28.7	38.3
	PCIe® Gen3 x16	2	4	4	6	3	4	0	0	1	1
	PCIe Gen3 x16/Gen4 x8 / CCIX[1]	–	–	–	–	–	–	8	4	–	–
	150G Interlaken	3	4	6	9	6	8	0	0	8	8
	100G Ethernet w/ KR4 RS-FEC	3	4	6	9	9	12	0	2	15	15
	Max. Single-Ended HP I/Os	520	832	832	832	624	832	1,976	572	676	676
	Max. Single-Ended HD I/Os	0	0	0	0	0	0	96	72	0	0
	GTY 32.75Gb/s Transceivers	40	80	80	120	96	128	80	34	32	32
	GTM 58Gb/s PAM4 Transceivers	–	–	–	–	–	–	–	4	48	48
	100G / 50G KP4 FEC	–	–	–	–	–	–	–	2 / 4	24 / 48	24 / 48
	Extended[2]	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3
	Industrial	-1 -2	-1 -2	-1 -2	-1 -2	-1 -2	-1 -2	–	-1, -2	-1 -2	-1 -2
[4, 5]	Footprint[3, 4, 5]	Dim. (mm)	HP I/O, GTY						HP I/O, HD I/O, GTY	HP I/O, HD I/O, GTY, GTM		
Footprint compatible with 20nm UltraScale Devices with same footprint identifier	A1365	35x35								364, 0, 34[8], 4		
	C1517	40x40	520, 40									
	J1760	42.5x42.5								572, 72, 34, 4		
	F1924[6]	45x45					624, 64					
	A2104	47.5x47.5		832, 52	832, 52	832, 52						
		52.5x52.5[7]						832, 52				
	B2104	47.5x47.5		702, 76	702, 76	702, 76	572, 76					
		52.5x52.5[7]						702, 76				
	C2104	47.5x47.5		416, 80	416, 80	416, 104	416, 96					
		52.5x52.5[7]						416, 104				
	D2104	47.5x47.5				676, 76	572, 76					
		52.5x52.5[7]						676, 76			676, 16, 30	676, 16, 30
	H2104	47.5x47.5										
	A2577	52.5x52.5				448, 120	448, 96	448, 128			448, 32, 48	448, 32, 48
	A3824	65x65							1976, 96,48			
	B3824	65x65							1664, 96, 80			

1. This block operates in compatibility mode for 16.0GT/s (Gen4) operation. See PG213.
2. -2LE (Tj = 0°C to 110°C). See Ordering Information in DS890.
3. For full part number details, see DS890, *UltraScale Architecture and Product Overview*.
4. All packages are 1.0mm ball pitch.
5. Consult UG583, *UltraScale Architecture PCB Design User Guide* for specific migration details.
6. The GTY transceiver line rate in the F1924 footprint is package limited to 16.3Gb/s. Refer to data sheet for details.
7. These 52.5x52.5mm packages have the same PCB ball footprint as the 47.5x47.5mm packages and are footprint compatible.
8. GTYs in quads 224-230 and 232 are limited to 16Gb/s.

Virtex® UltraScale+™ HBM FPGAs

	HBM (4GB)	HBM (8GB)			HBM (16GB)		
Device Name	VU31P	VU33P	VU35P	VU37P	VU45P	VU47P	VU57P
System Logic Cells (K)	962	962	1,907	2,852	1,907	2,852	2,852
CLB Flip-Flops (K)	879	879	1,743	2,607	1,743	2,607	2,607
CLB LUTs (K)	440	440	872	1,304	872	1,304	1,304
Max. Dist. RAM (Mb)	12.5	12.5	24.6	36.7	24.6	36.7	36.7
Total Block RAM (Mb)	23.6	23.6	47.3	70.9	47.3	70.9	70.9
UltraRAM (Mb)	90.0	90.0	180.0	270.0	180.0	270.0	270.0
HBM DRAM (GB)	4	8	8	8	16	16	16
HBM AXI Interfaces	32	32	32	32	32	32	32
Clock Mgmt Tiles (CMTs)	4	4	8	12	8	12	12
DSP Slices	2,880	2,880	5,952	9,024	5,952	9,024	9,024
Peak INT8 DSP (TOP/s)	8.9	8.9	18.6	28.1	18.6	28.1	28.1
PCIe® Gen3 x16	0	0	1	2	1	2	0
PCIe Gen3 x16/Gen4 x8 / CCIX(1)	4	4	4	4	4	4	4
150G Interlaken	0	0	2	4	2	4	4
100G Ethernet w/ KR4 RS-FEC	2	2	5	8	5	8	10
Max. Single-Ended HP I/Os	208	208	416	624	416	624	624
GTY 32.75Gb/s Transceivers	32	32	64	96	64	96	32
GTM 58Gb/s PAM4 Transceivers	–	–	–	–	–	–	32
100G / 50G KP4 FEC	–	–	–	–	–	–	16/32
Extended(2)	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3
Industrial	–	–	–	–	–	–	–

Footprint(3, 4, 5, 6)	Dim. (mm)	HP I/O, GTY						HP I/O, GTY, GTM
H1924	45x45	208, 32						
H2104	47.5x47.5		208, 32	416, 64		416, 64		
H2892	55x55			416, 64	624, 96	416, 64	624, 96	
K2892	55x55							624, 32, 32

1. This block operates in compatibility mode for 16.0GT/s (Gen4) operation. See PG213.
2. -2LE (Tj = 0°C to 110°C). See Ordering Information in DS890.
3. For full part number details, see DS890, *UltraScale Architecture and Product Overview*.
4. All packages are 1.0mm ball pitch.
5. Consult UG583, *UltraScale Architecture PCB Design User Guide* for specific migration details.
6. Footprint compatible with 20nm UltraScale Devices with same footprint identifier.

Virtex® UltraScale+™ FPGAs

Kintex® UltraScale+™ FPGAs

	Device Name	KU3P	KU5P	KU9P	KU11P	KU13P	KU15P	KU19P
Logic	System Logic Cells (K)	356	475	600	653	747	1,143	1,843
	CLB Flip-Flops (K)	325	434	548	597	683	1,045	1,685
	CLB LUTs (K)	163	217	274	299	341	523	842
Memory	Max. Distributed RAM (Mb)	4.7	6.1	8.8	9.1	11.3	9.8	11.6
	Total Block RAM (Mb)	12.7	16.9	32.1	21.1	26.2	34.6	60.8
	UltraRAM (Mb)	13.5	18.0	0	22.5	31.5	36.0	81.0
Clocking	Clock Mgmt Tiles (CMTs)	4	4	4	8	4	11	9
Integrated IP	DSP Slices	1,368	1,824	2,520	2,928	3,528	1,968	1,080
	PCIE4 (PCIe® Gen3 x16)	1	1	0	4	0	5	0
	PCIE4C (PCIe® Gen3 x16 / Gen4 x8 /CCIX)	0	0	0	0	0	0	3
	150G Interlaken	0	0	0	1	0	4	0
	100G Ethernet w/RS-FEC	0	1	0	2	0	4	1
I/O	Max. Single-Ended HD I/Os	96	96	96	96	96	96	72
	Max. Single-Ended HP I/Os	208	208	208	416	208	572	468
	GTH 16.3Gb/s Transceivers	0	0	28	32	28	44	0
	GTY 32.75Gb/s Transceivers	16	16	0	20	0	32	32
Speed Grades	Extended[1]	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3
	Industrial	-1 -1L -2	-1 -1L -2	-1 -1L -2	-1 -1L -2	-1 -1L -2	-1 -1L -2	-1 -1L -2
Footprint compatible with 20nm UltraScale Devices with same footprint identifier	Footprint[2, 3]	Dimensions (mm)	HD I/O, HP I/O, GTH 16.3Gb/s, GTY 32.75Gb/s						
	B784[4]	23x23[5]	96, 208, 0, 16	96, 208, 0, 16					
	A676[4]	27x27	48, 208, 0, 16	48, 208, 0, 16					
	B676	27x27	72, 208, 0, 16	72, 208, 0, 16					
	D900[4]	31x31	96, 208, 0, 16	96, 208, 0, 16		96, 312, 16, 0			
	E900	31x31			96, 208, 28, 0		96, 208, 28, 0		
	A1156[4]	35x35				48, 416, 20, 8		48, 468, 20, 8	
	E1517	40x40				96, 416, 32, 20		96, 416, 32, 24	
	A1760	42.5x42.5						96, 416, 44, 32	
	E1760	42.5x42.5						96, 572, 32, 24	
	J1760	42.5x42.5							72, 468, 0, 32
	B2104	47.5x47.5							72, 468, 0, 32

1. -2LE (Tj = 0°C to 110°C). For more details, see the Ordering Information section in DS890, UltraScale Architecture and Product Overview.
2. Maximum achievable performance is device and package dependent; consult the associated data sheet for details.
3. For full part number details, see the Ordering Information section in DS890, *UltraScale Architecture and Product* Overview.
4. GTY transceiver line rates are package limited: B784 to 12.5 Gb/s; A676, D900, and A1156 to 16.3 Gb/s. Refer to data sheet for details.
5. The B784 package is only offered in 0.8mm ball pitch. All other packages are 1.0mm ball pitch.

Artix® UltraScale+™ FPGAs

Device Name	AU10P	AU15P	AU20P	AU25P
System Logic Cells (K)	96	170	238	308
CLB Flip-Flops (K)	88	156	218	282
CLB LUTs (K)	44	78	109	141
Max. Dist. RAM (Mb)	1.0	2.5	3.2	4.7
Total Block RAM (Mb)	3.5	5.1	7.0	10.5
36K Block RAM Blocks	100	144	200	300
UltraRAM (Mb)	–	–	–	–
Clock Management Tiles (CMTs)	3	3	3	4
DSP Slices	400	576	900	1,200
PCIe® Gen3 / Gen4	PCIe Gen 4	PCIe Gen 4	PCIe Gen 3	PCIe Gen 3
AMS - System Monitor	1	1	1	1
Max. Single-Ended HD I/Os	72	72	72	96
Max. Single-Ended HP I/Os	156	156	156	208
GTH 16.3Gb/s Transceivers[1]	12	12	–	–
GTY 16.3Gb/s Transceivers[1]	–	–	12	12
Extended	-1 -2			
Industrial	-1 -2 -1L			

Footprint[2,3]	Dim. (mm)	Ball Pitch (mm)	HD I/O, HP I/O, GTH, GTY			
A368	11.5x9.5	0.5	24, 104, 8, 0	24, 104, 8, 0		
B484	19x19	0.8	48, 156, 12, 0	48, 156, 12, 0		
B784	23x23	0.8			72, 156, 0, 12	96, 208, 0, 12
B676	27x27	1.0	72, 156, 12, 0	72, 156, 12, 0	72, 156, 0, 12	72, 208, 0, 12

1. GTH and GTY transceiver line rates are package limited: SFVB784, SBVB484, and UBVA368 to 12.5Gb/s.12.5Gb/s operation in UBVA368 package is pending characterization.
2. For full part number details, see DS890, *UltraScale Architecture and Product Overview*.
3. Consult UG583, *UltraScale Architecture PCB Design User Guide* for specific migration details.