DATAFLOW CODE GENERATION FOR FPGA

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Work in progress

Hardware acceleration for HPC / embedded

- High throughput / low latency
- Low energy

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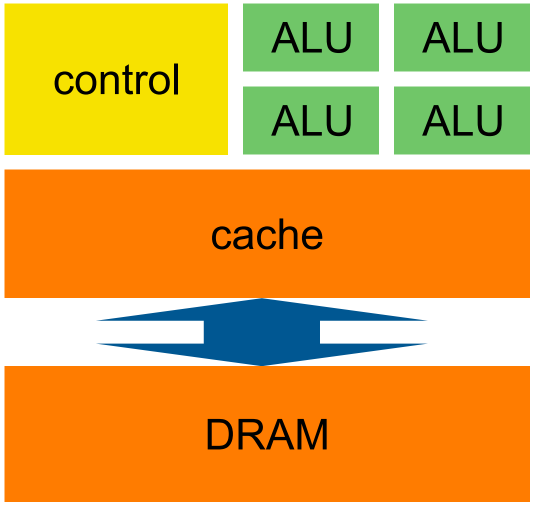
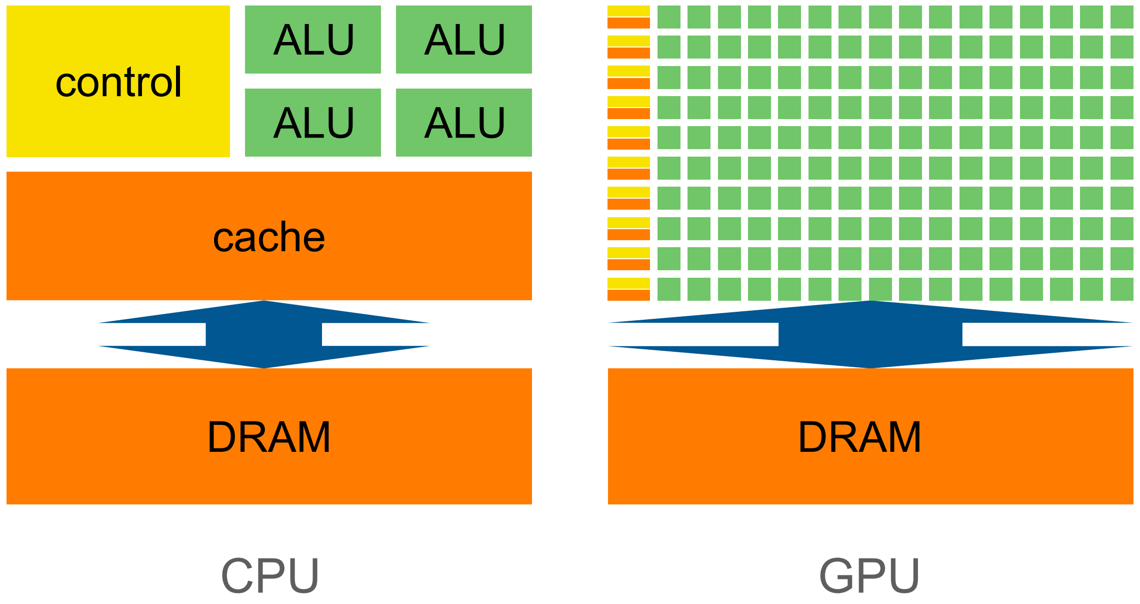


CPU

Hardware acceleration for HPC / embedded

- High throughput / low latency
- Low energy



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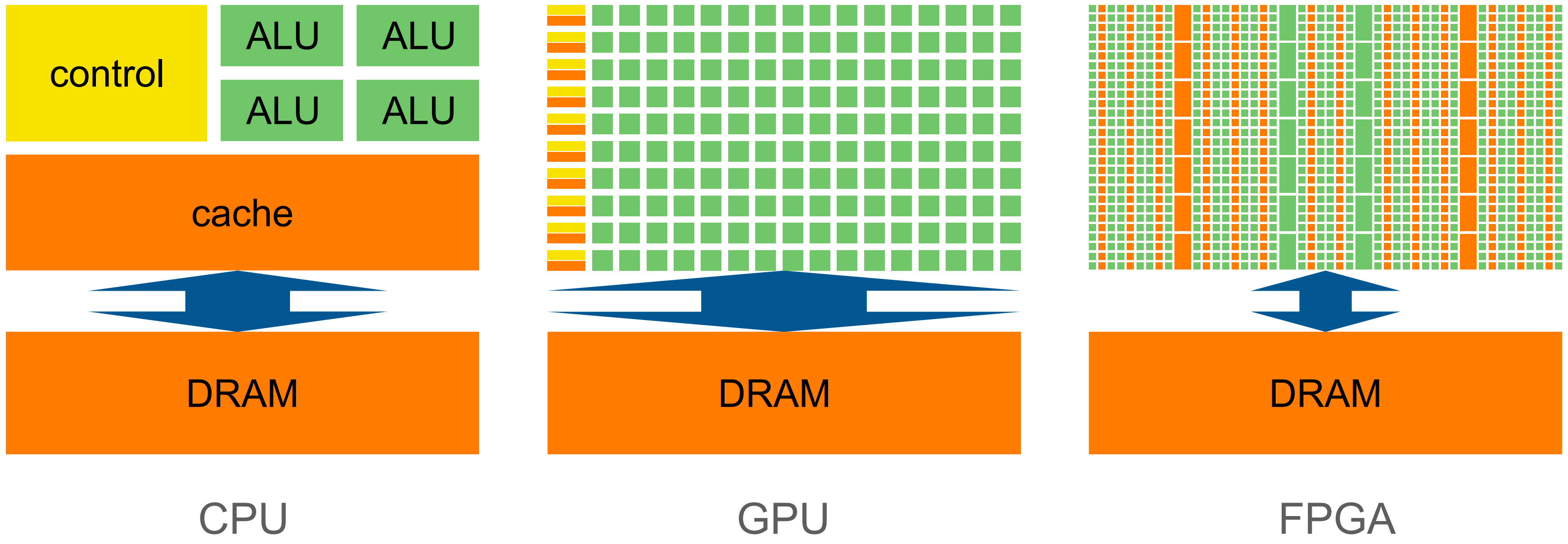
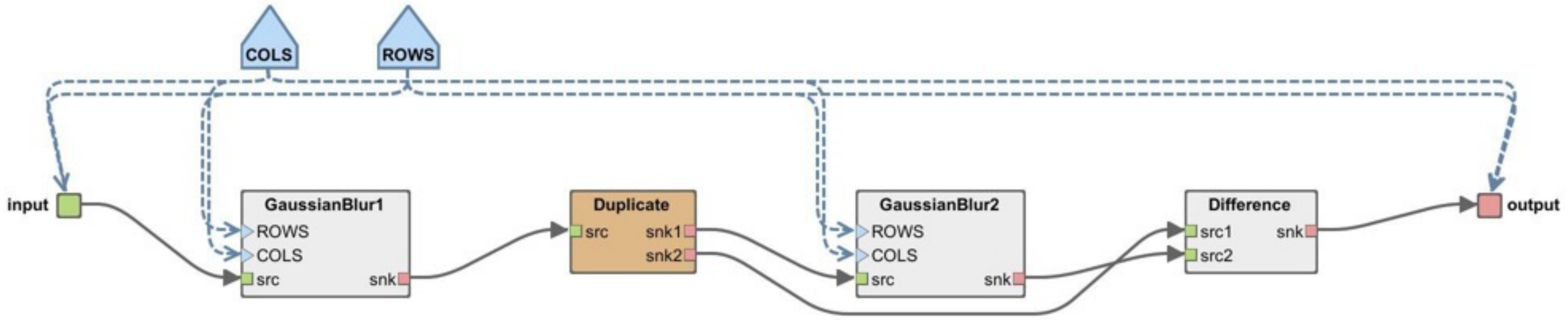


Dataflow programming

- Natural expression for signal and image processing



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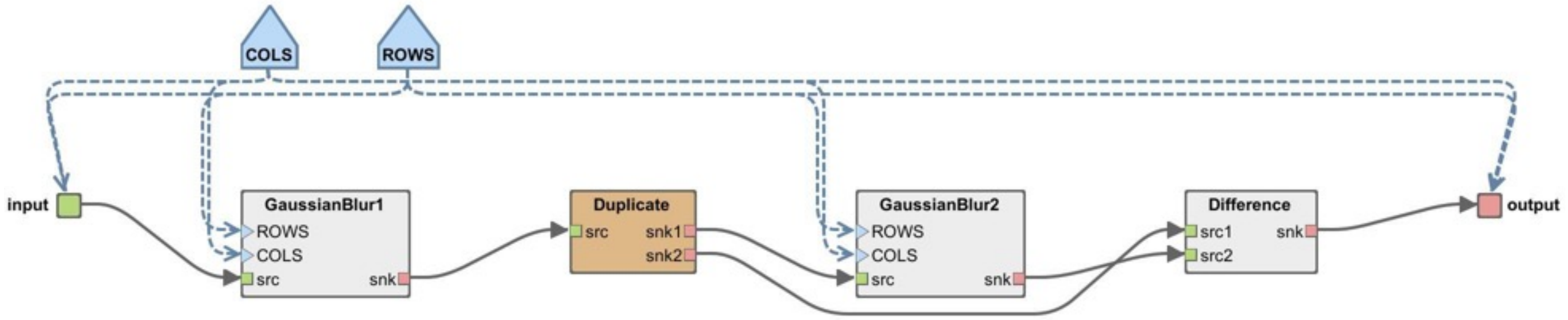

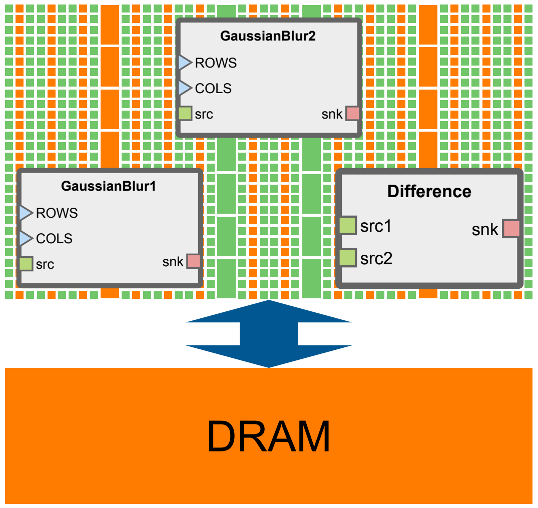

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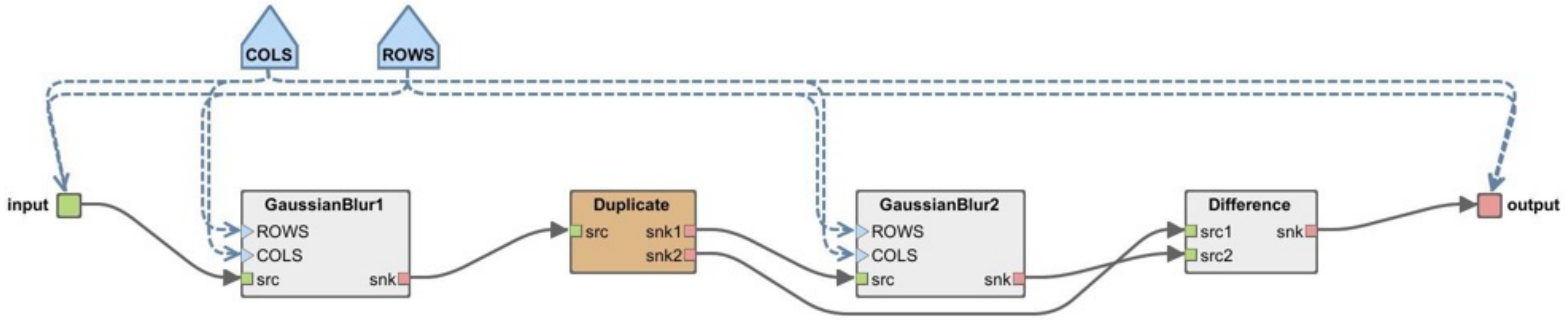

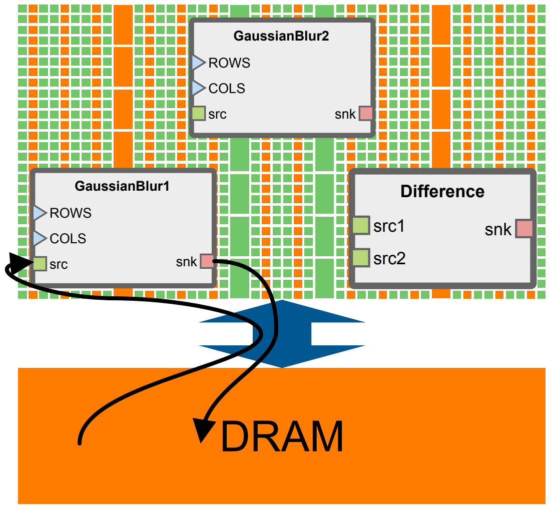

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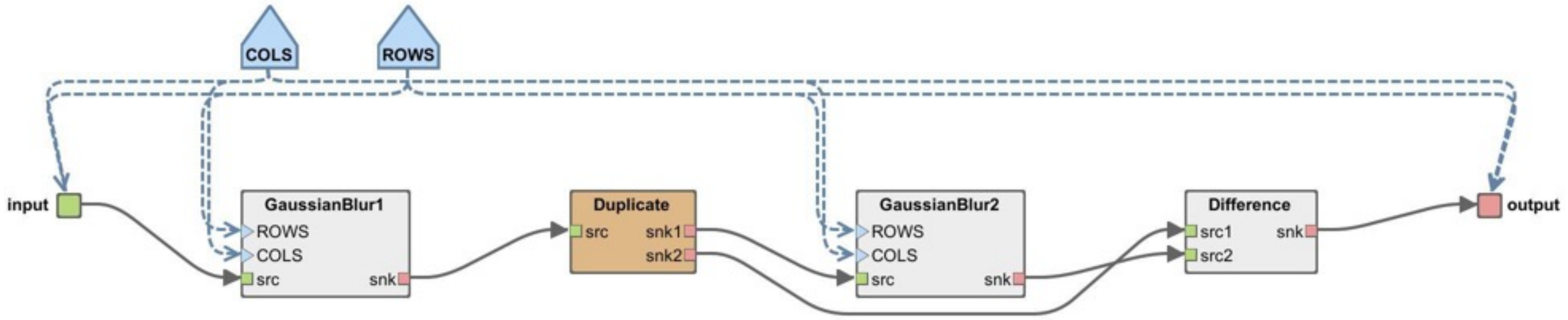
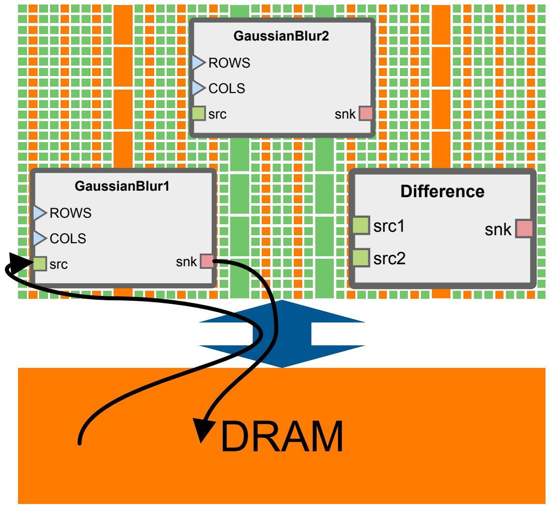
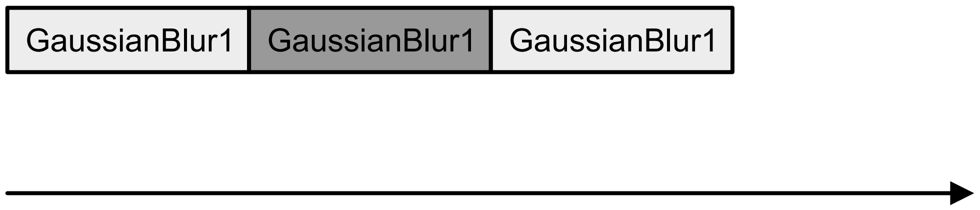




- High throughput



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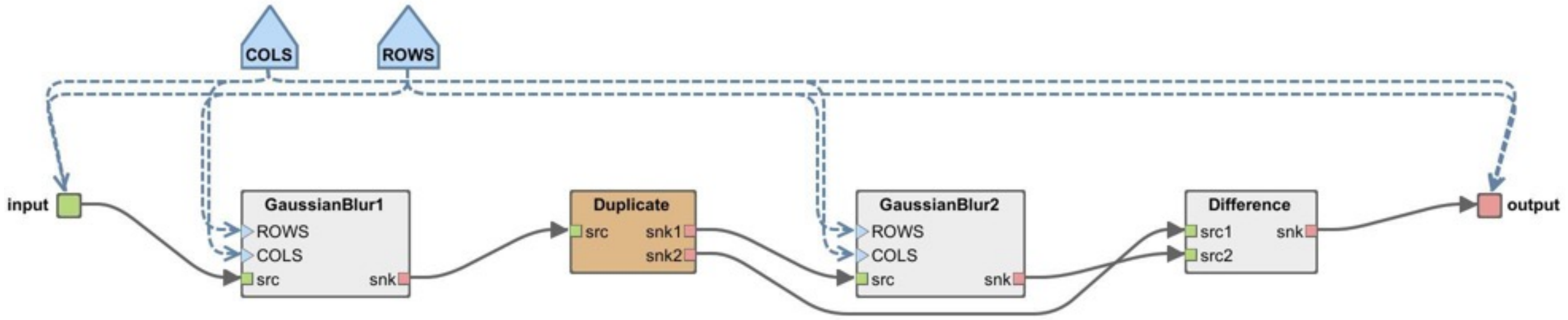
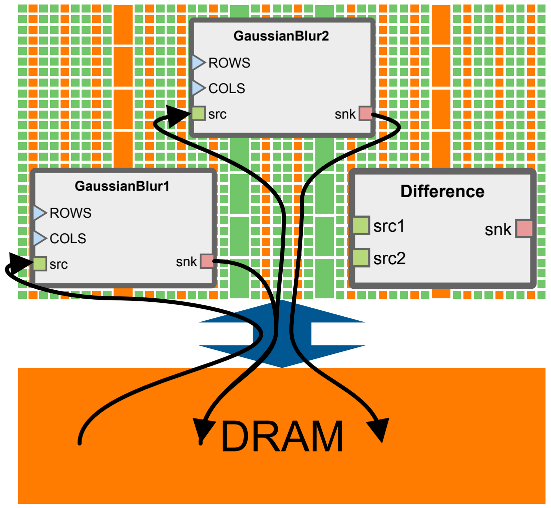
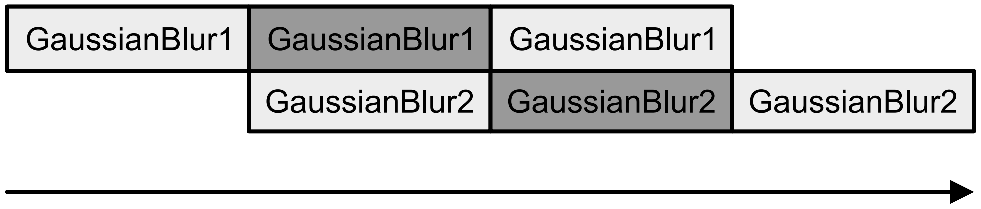




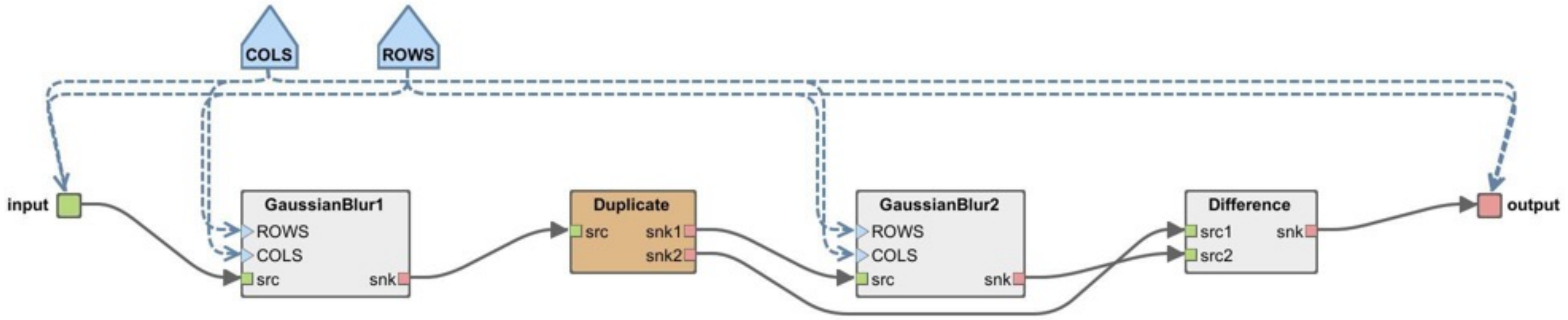
- High throughput
- High memory usage

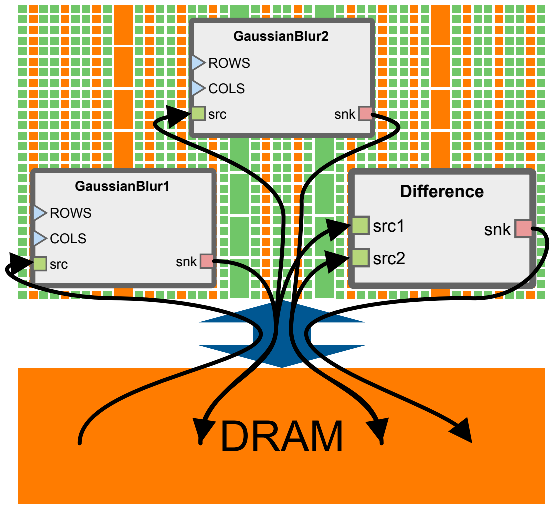


GaussianBlur1	GaussianBlur1	GaussianBlur1	
	GaussianBlur2	GaussianBlur2	GaussianBlur2

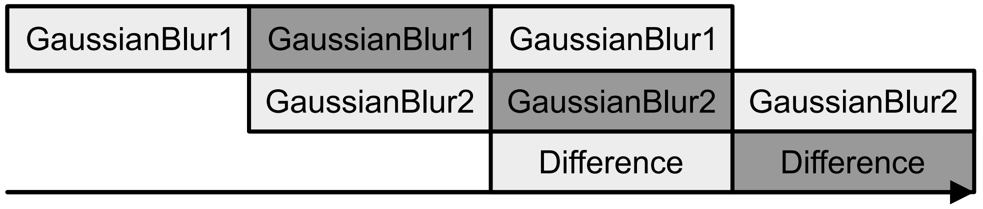
Dataflow programming

- Natural expression for signal and image processing





- High throughput
- High memory usage
- High bandwidth usage
- Long latency



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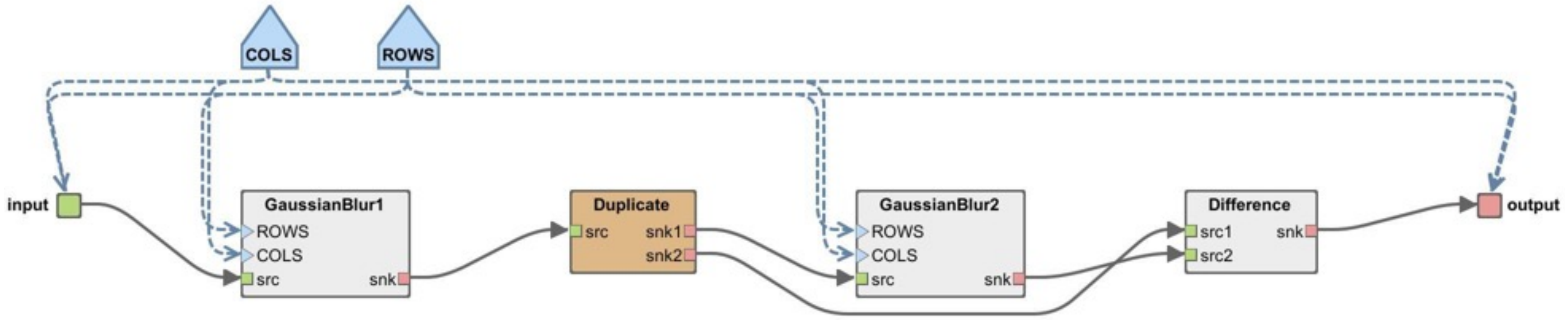

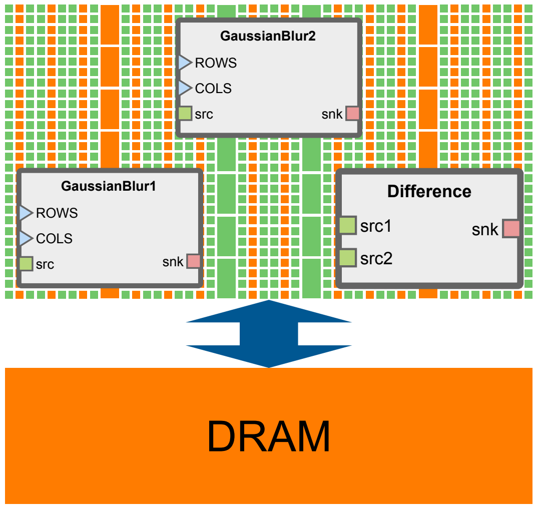

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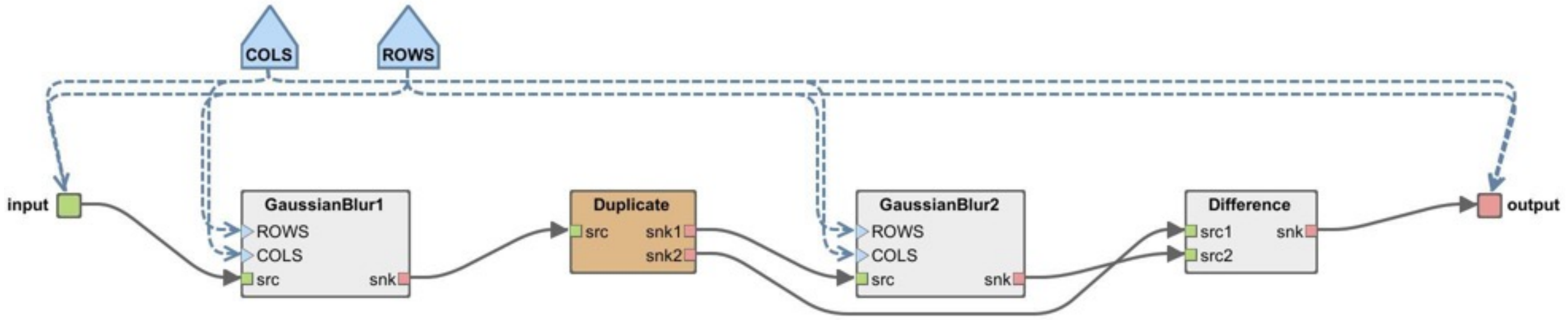
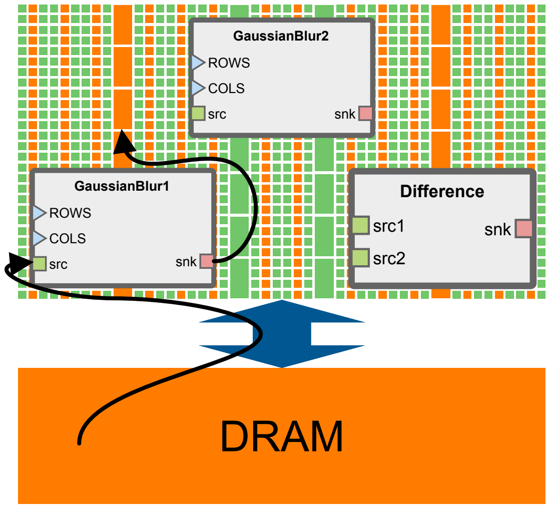
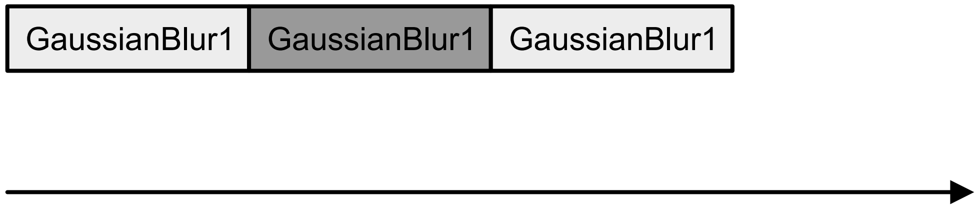




- High throughput



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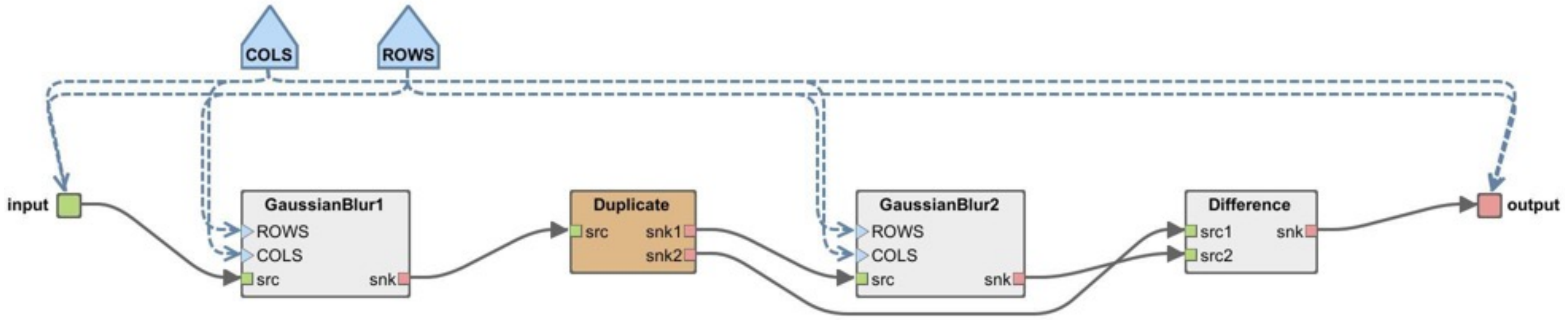
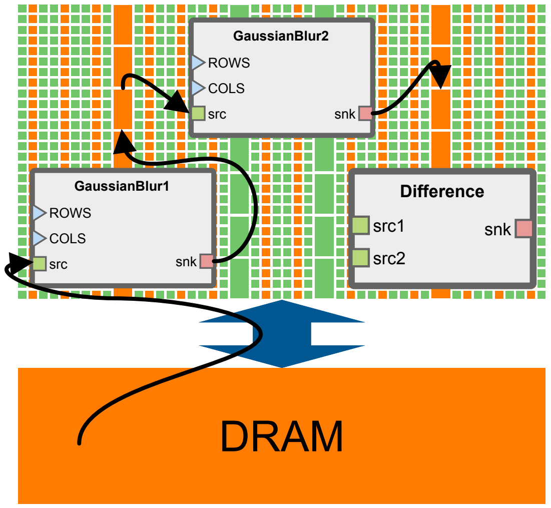
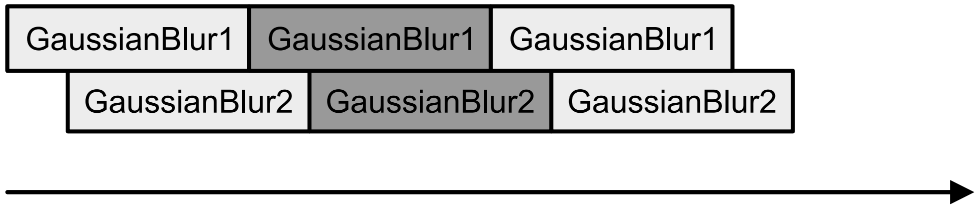




- High throughput
- Low memory usage



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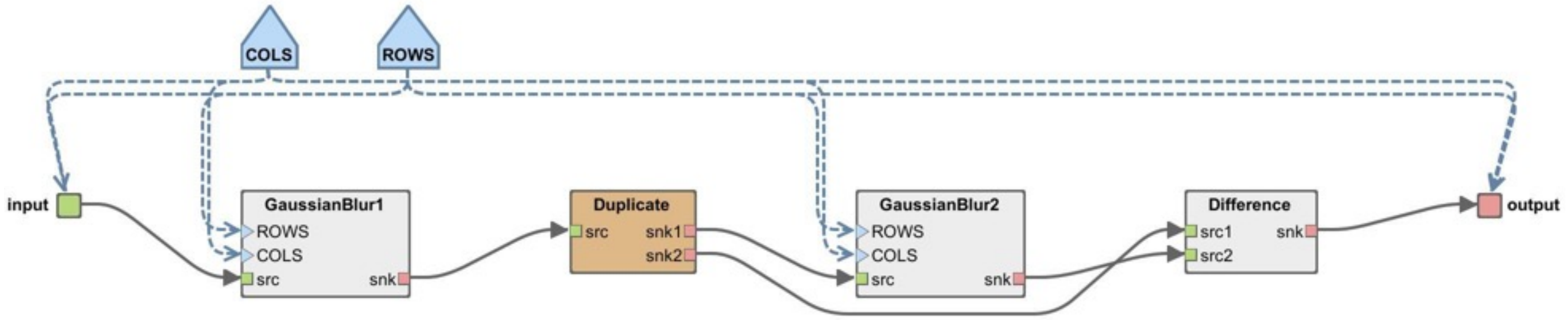

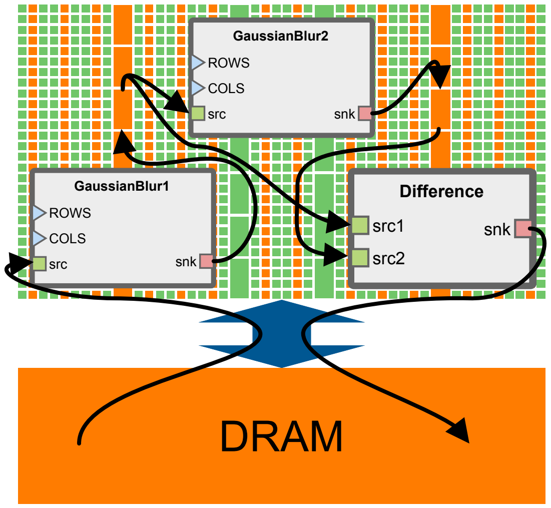

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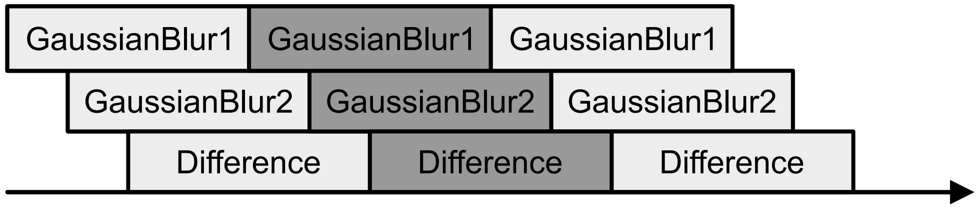
- Low memory usage
- Low bandwidth usage
- Low latency



Dataflow programming

- Natural expression for signal and image processing
- Pipeline implementation good match for FPGA

Dataflow programming

- Natural expression for signal and image processing
- Pipeline implementation good match for FPGA
- Native support in Vitis HLS

```
void top_graph(hls::stream<int> &input, hls::stream<int> &output) {
// FIFOs
  static hls::stream<int> GaussianBlur1ToDuplicate;
#pragma HLS stream variable=GaussianBlur1ToDuplicate depth=2
  static hls::stream<int> DuplicateToDifference;
#pragma HLS stream variable=DuplicateToDifference depth=N
  // …
  // Kernels
#pragma HLS DATAFLOW
  GaussianBlur1(input, GaussianBlur1ToDuplicate);
  Duplicate(GaussianBlur1ToDuplicate, DuplicateToGaussianBlur2,
DuplicateToDifference);
  GaussianBlur2(DuplicateToGaussianBlur2, GaussianBlur2ToDifference);
  Difference(GaussianBlur2ToDifference, DuplicateToDifference,
output);
}
```

Challenge for design productivity

- Express dataflow at high level
- Optimized hardware implementation

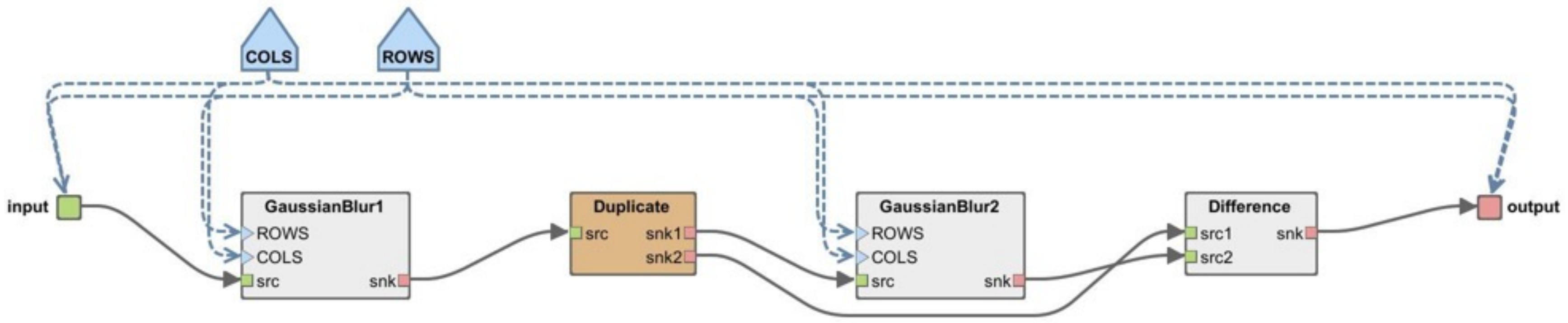
Problem statement

Challenge for design productivity

- Express dataflow at high level
- Optimized hardware implementation

Contributions

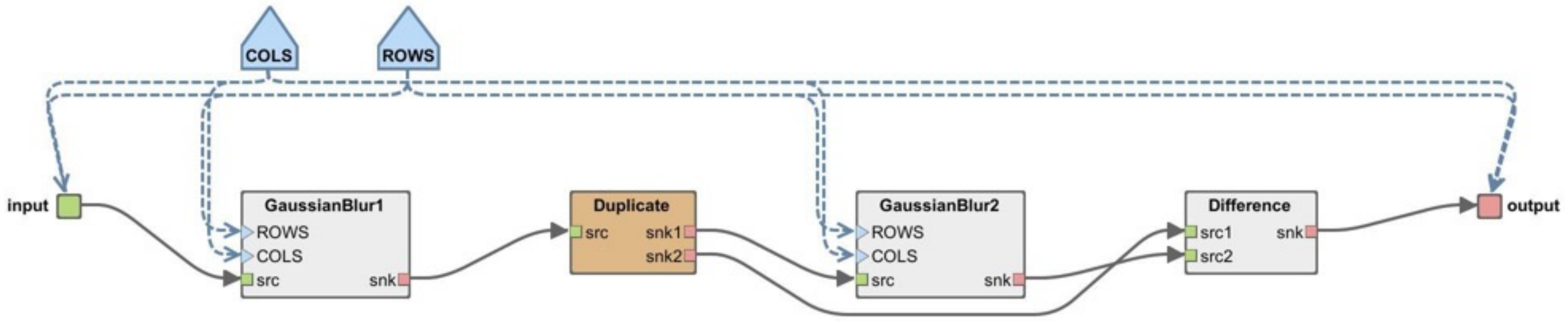
- Dataflow code generation for FPGA using HLS
- Automatic scheduling and buffer sizing
- Open source implementation in PREESM



https://preesm.github.io

DATAFLOW CODE GENERATION FOR FPGA USING HLS

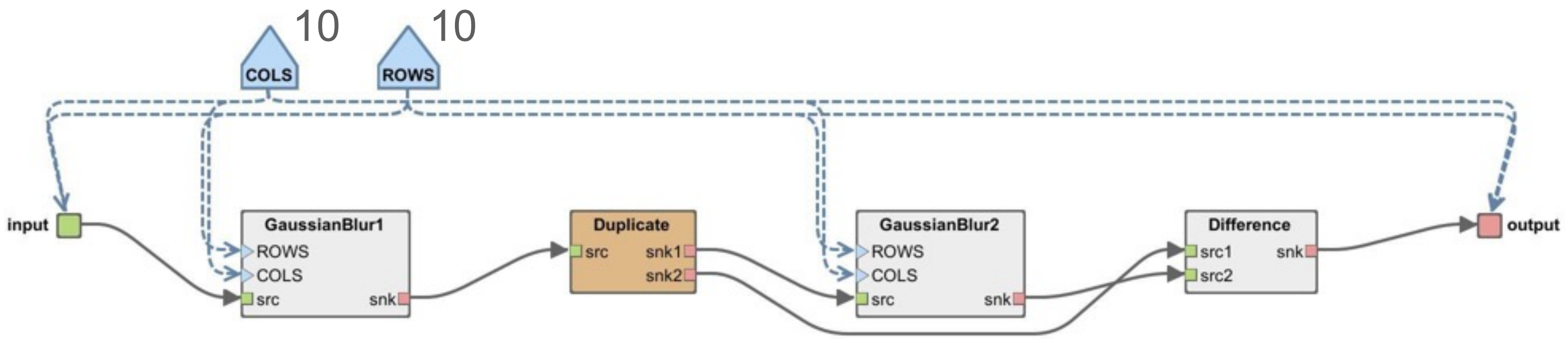
PiSDF graph based on PREESM



Dataflow definition

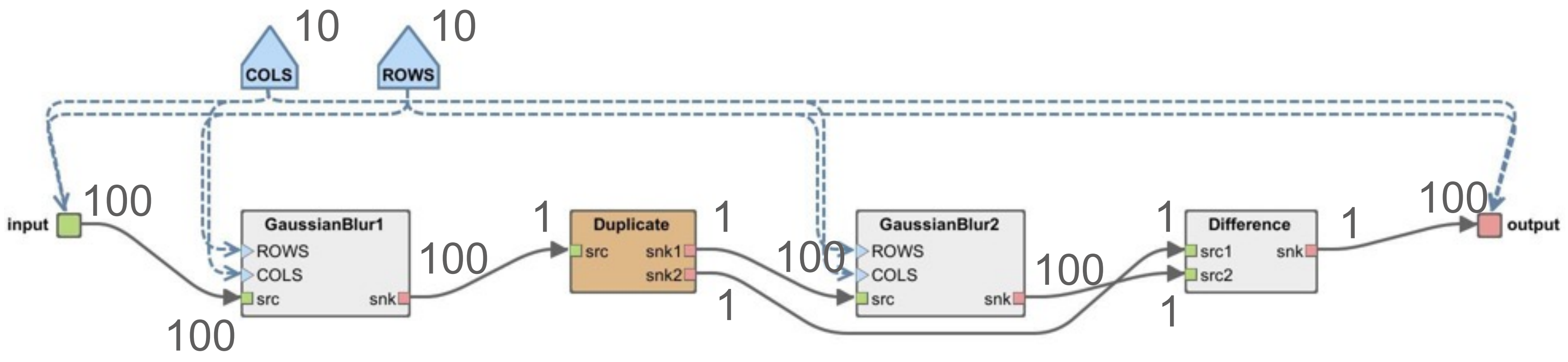
PiSDF graph based on PREESM

- **Parameterized**
- **Interfaced**
- **Synchronous Dataflow**



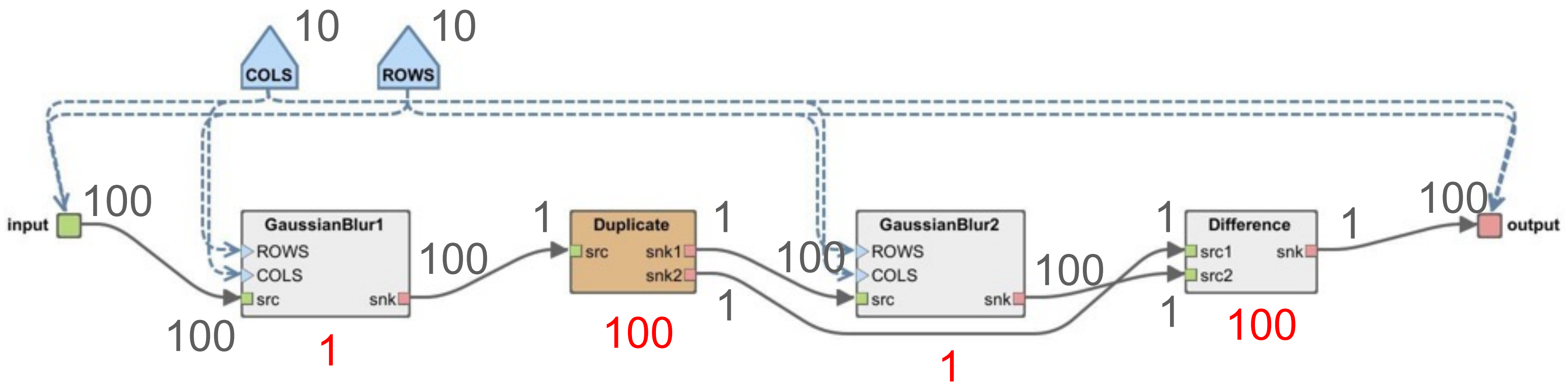
PiSDF graph based on PREESM

- Parameterized
- Interfaced
- Synchronous Dataflow
    - Multirate

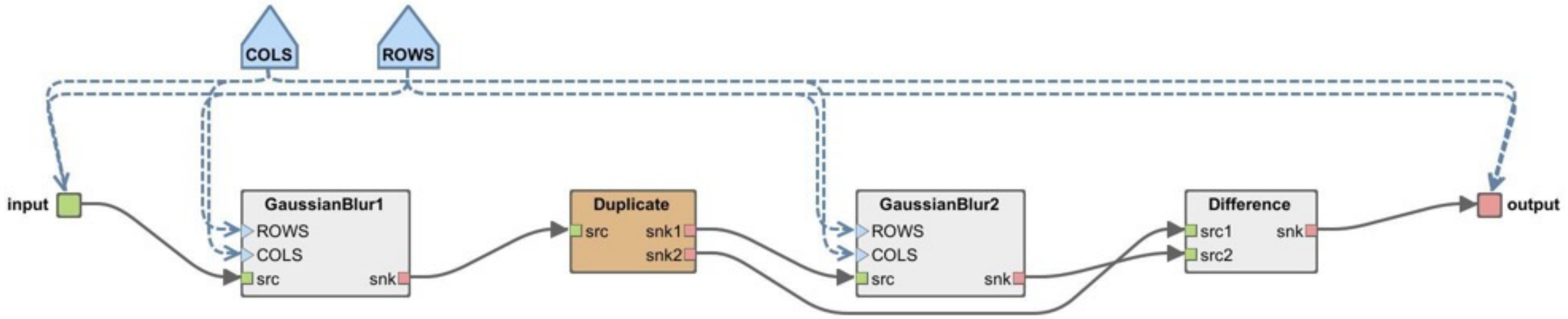


PiSDF graph based on PREESM

- **Parameterized**
- **Interfaced**
- **Synchronous Dataflow**
  - Multirate
  - Repetition factor
  - Deadlock free
  - Automatic scheduling and buffer sizing



Dataflow using HLS



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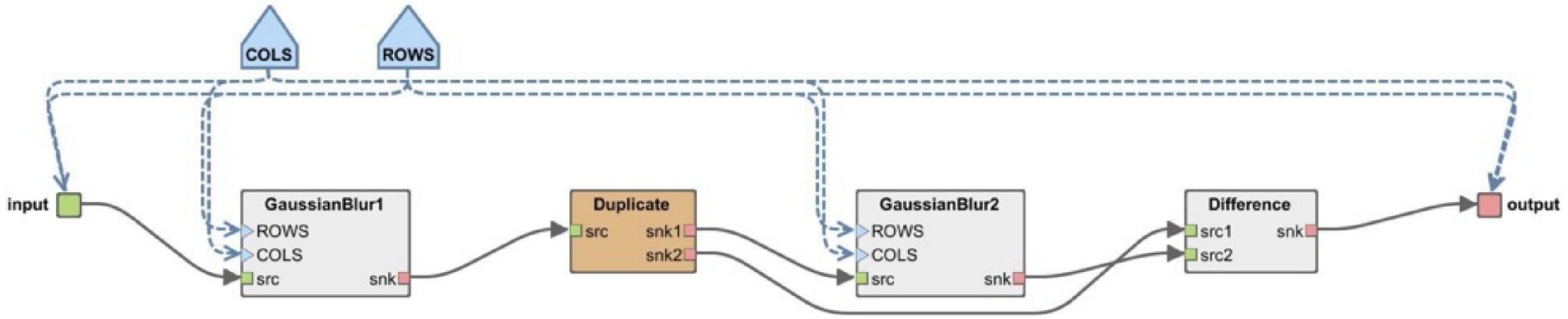
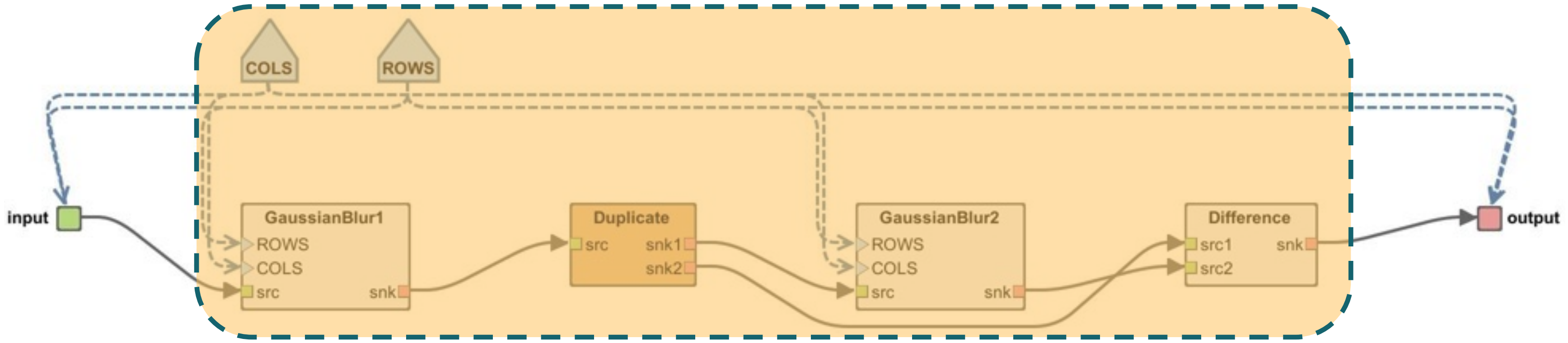


User provided

- **Kernels**
  - HLS
  - FIFO interface (stream<T>)

Dataflow using HLS



Kernels + Graph

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Code generation

- **Graph**
  - Multirate
  - Cyclic
  - Self-scheduled ASAP

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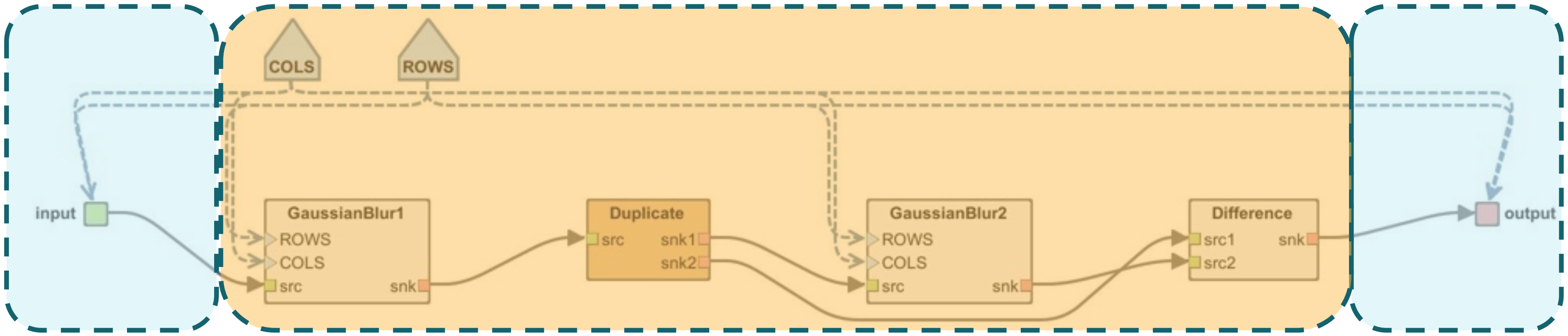

Input

Kernels + Graph

Output

User provided

- **Kernels**
  - HLS
  - FIFO interface (stream<T>)

- **Input / output**
  - Array interface (T*)
  - Batch transfer from/to RAM
  - Scheduled by host

Code generation

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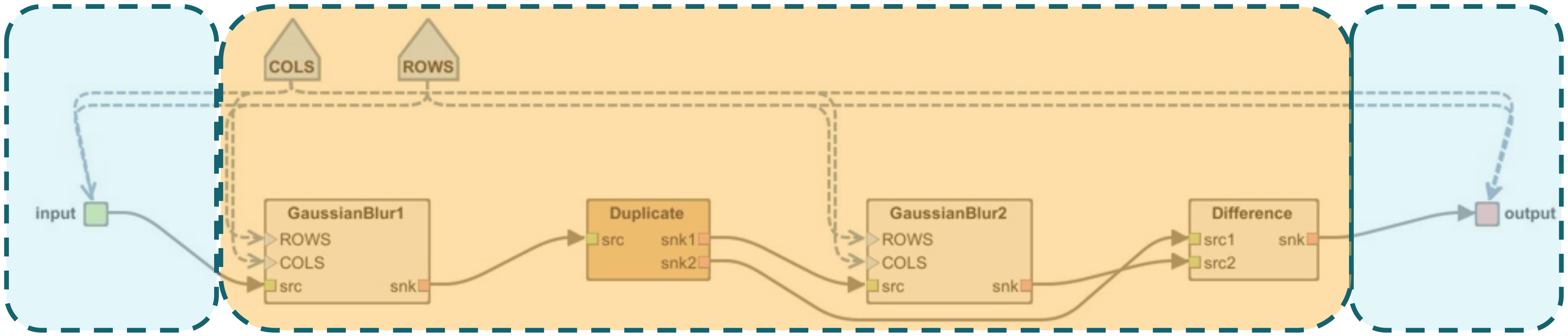
Dataflow using HLS



Input   Kernels + Graph   Output

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- **Input / output**
  - Array interface (T*)
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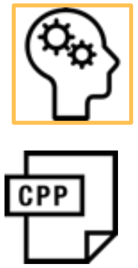
  - Scheduled by host
- **Host code**
  - OpenCL
  - PYNQ
  - Bare metal
  - Testbench

Compilation flow



Kernels

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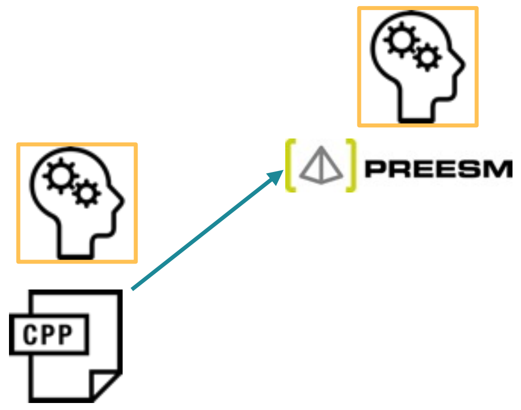

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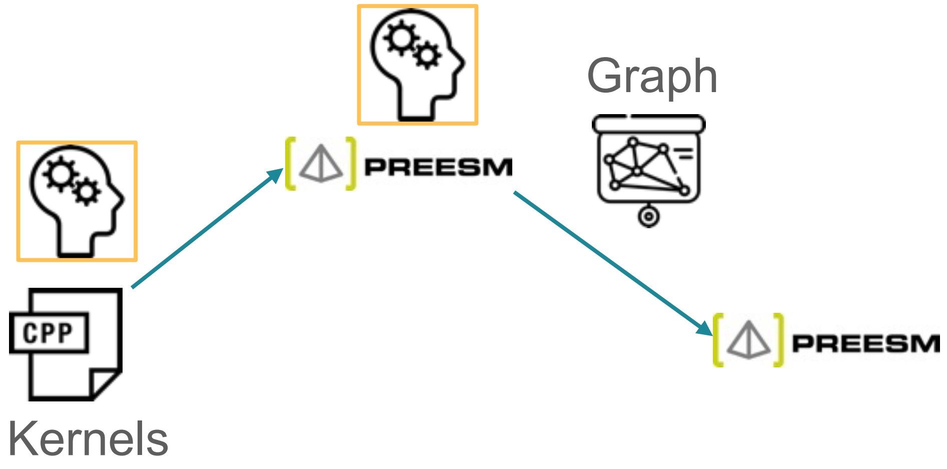

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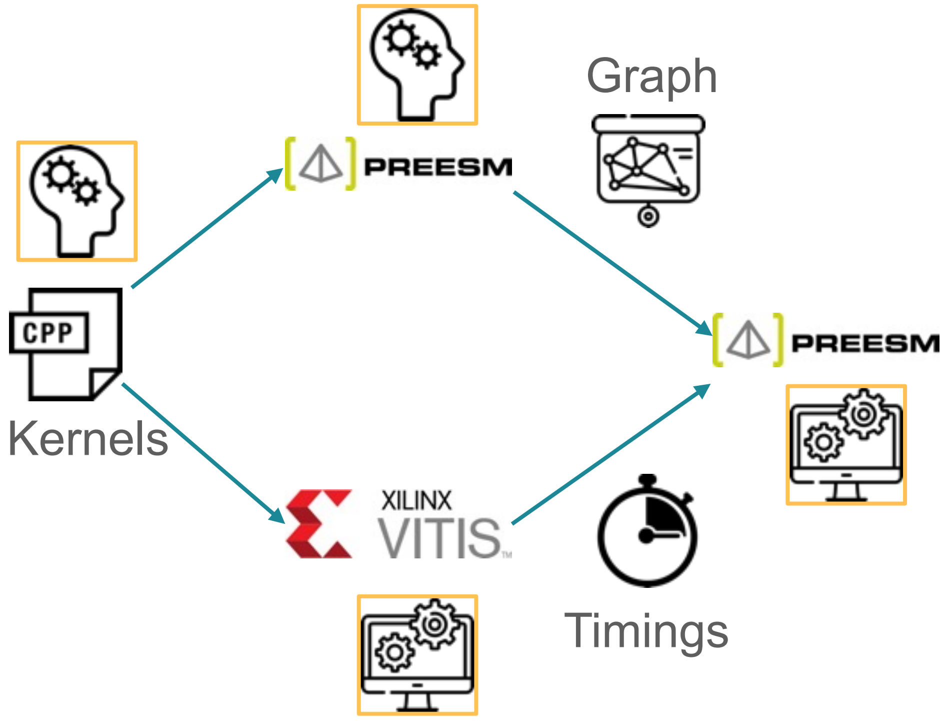

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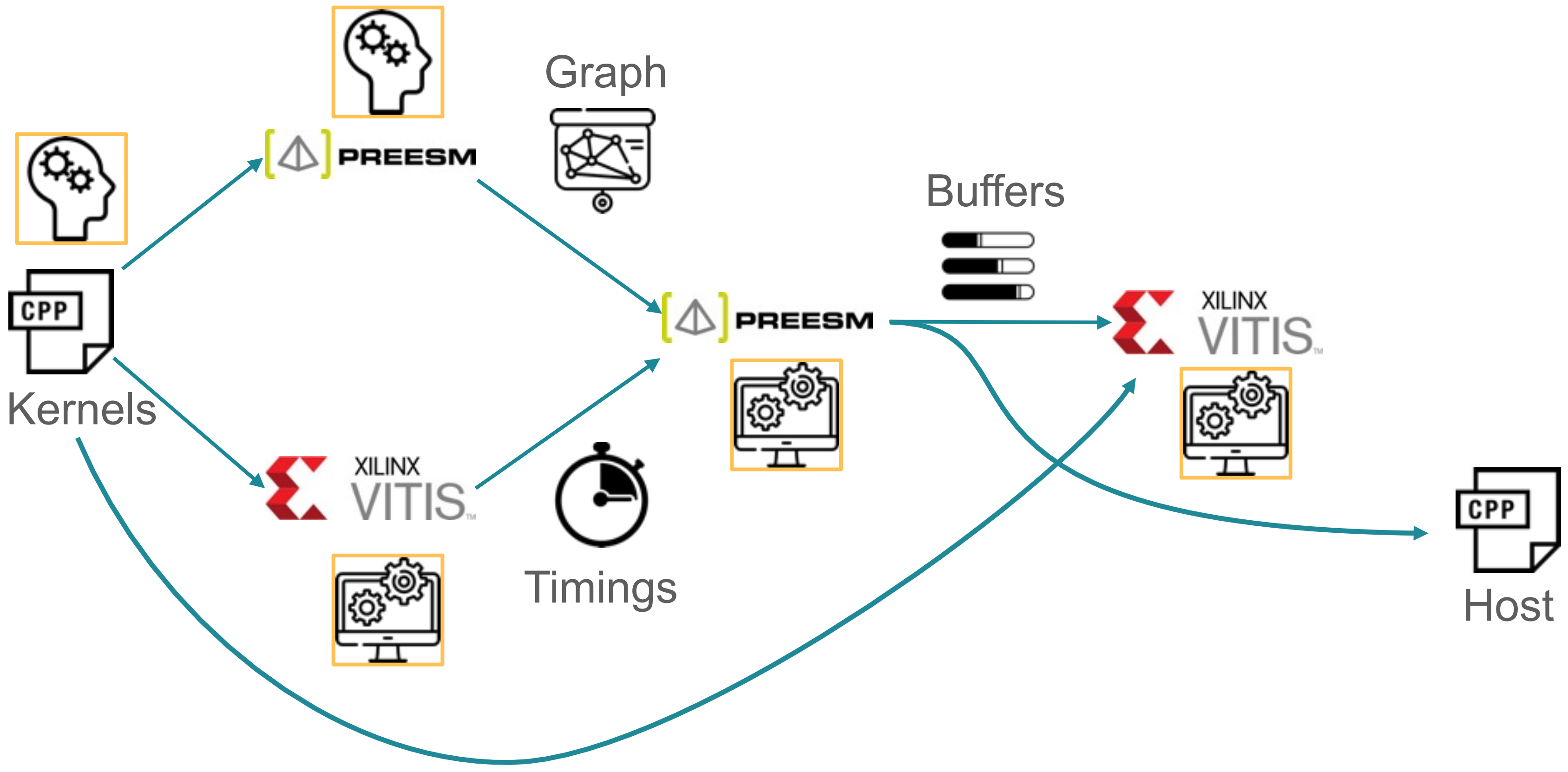

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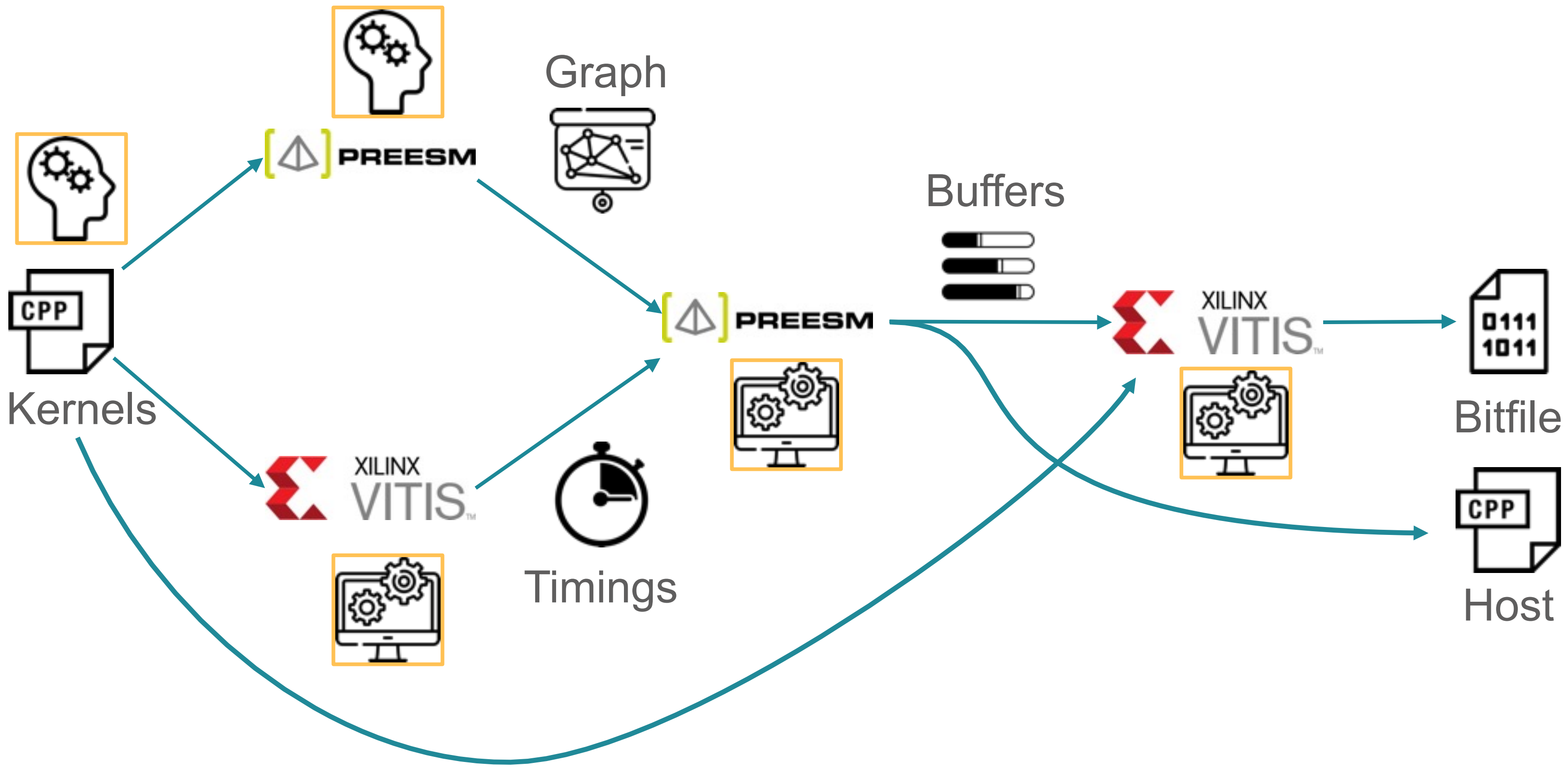
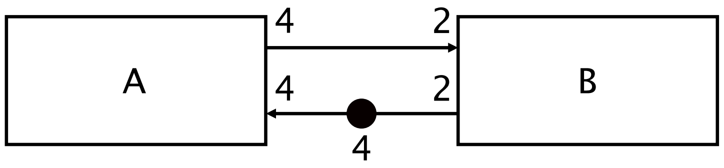


AUTOMATIC SCHEDULING AND BUFFER SIZING

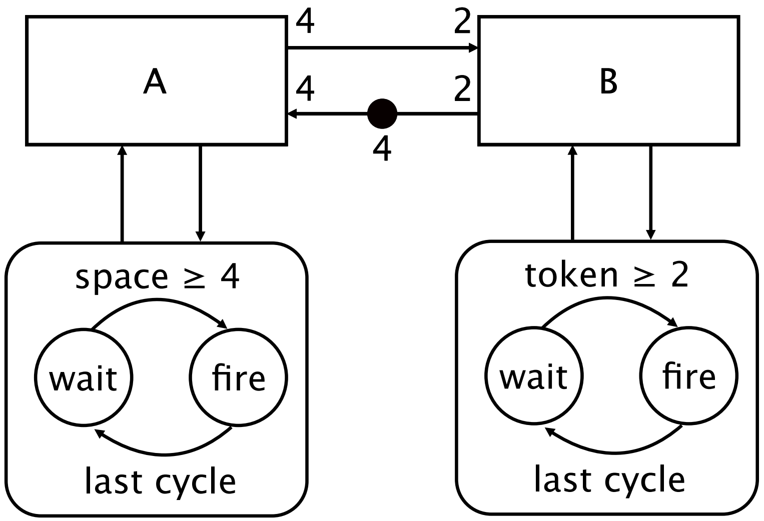
Problem: matching actor and hardware execution model



Problem: matching actor and hardware execution model

Acquire – Release

- Shared memory sync.



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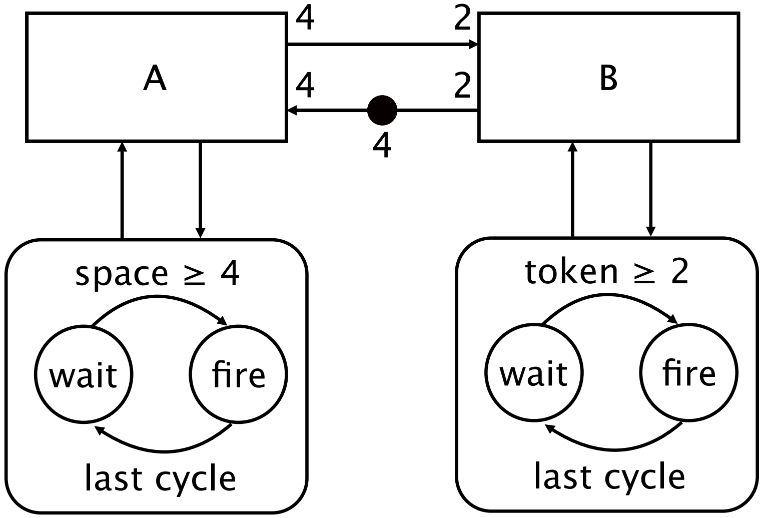

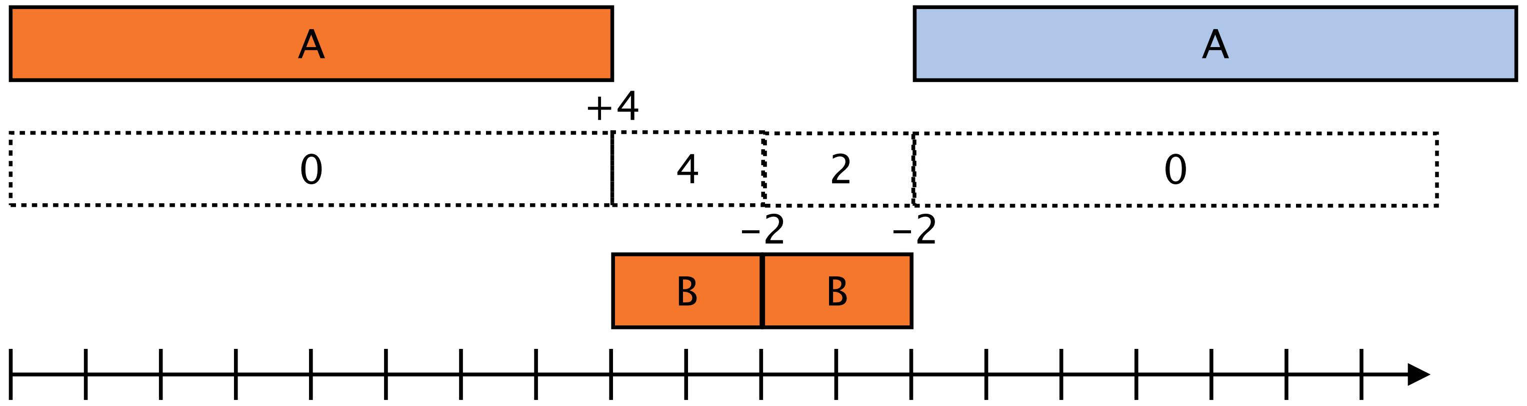

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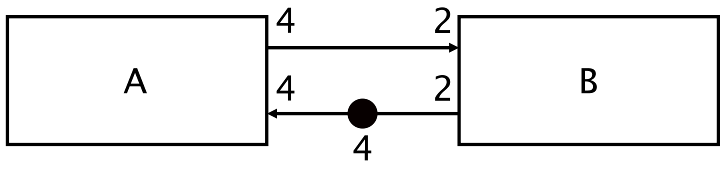

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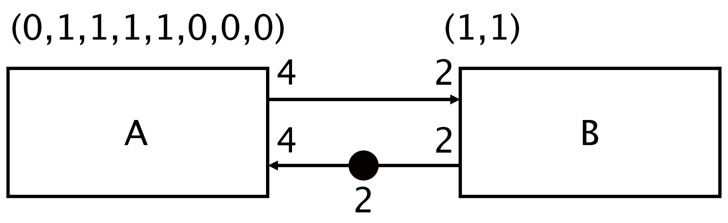
SDF Access Pattern [Tripakis et al. 11]

- Cycle accurate info
- Scalability issues



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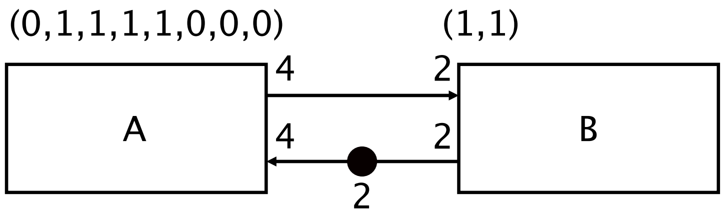

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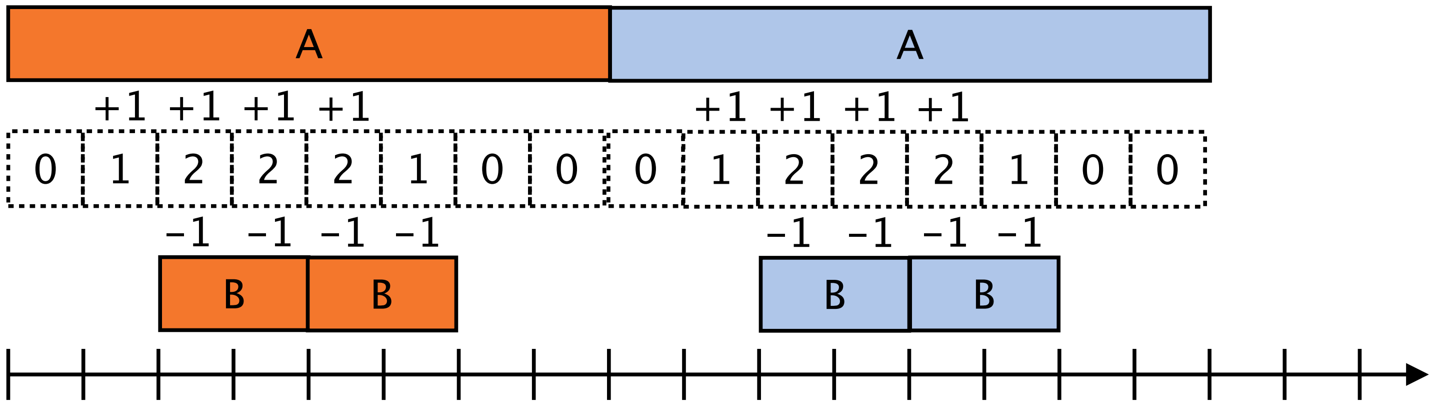

Affine approximation

Metrics:

- $\tau_p = 4\ tokens\ per\ execution$
- $II = 8\ cycles$
- $a_p = 0.5\ token/cycle$

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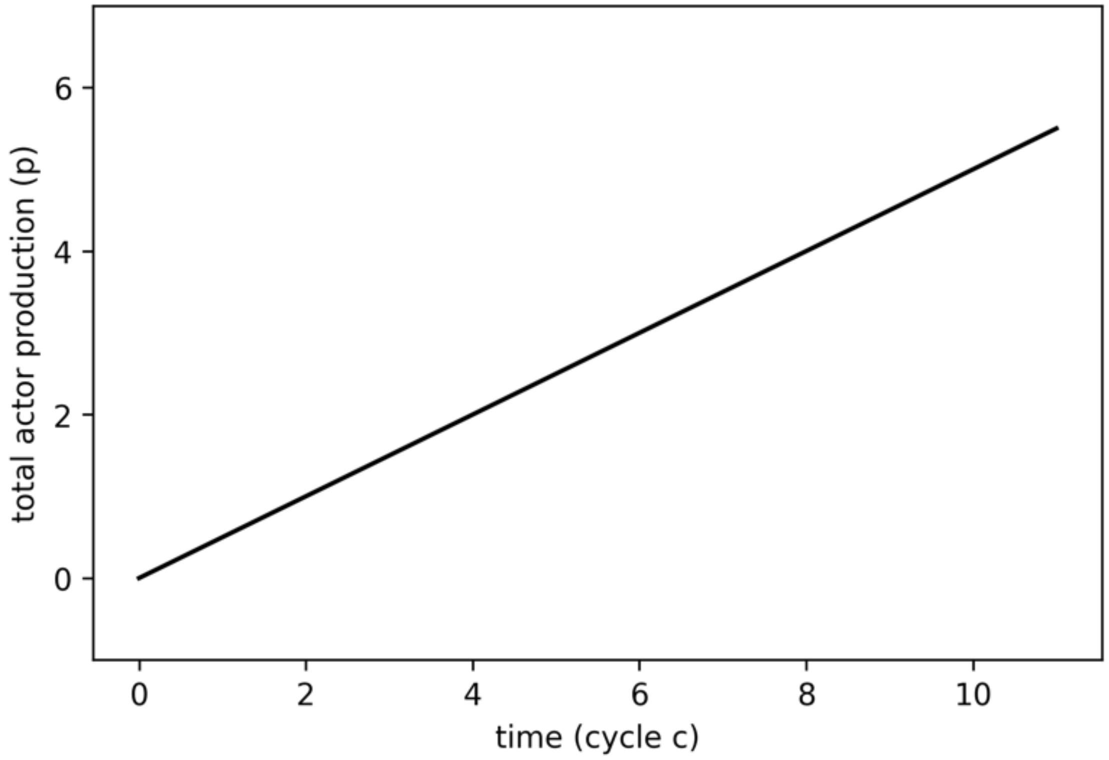

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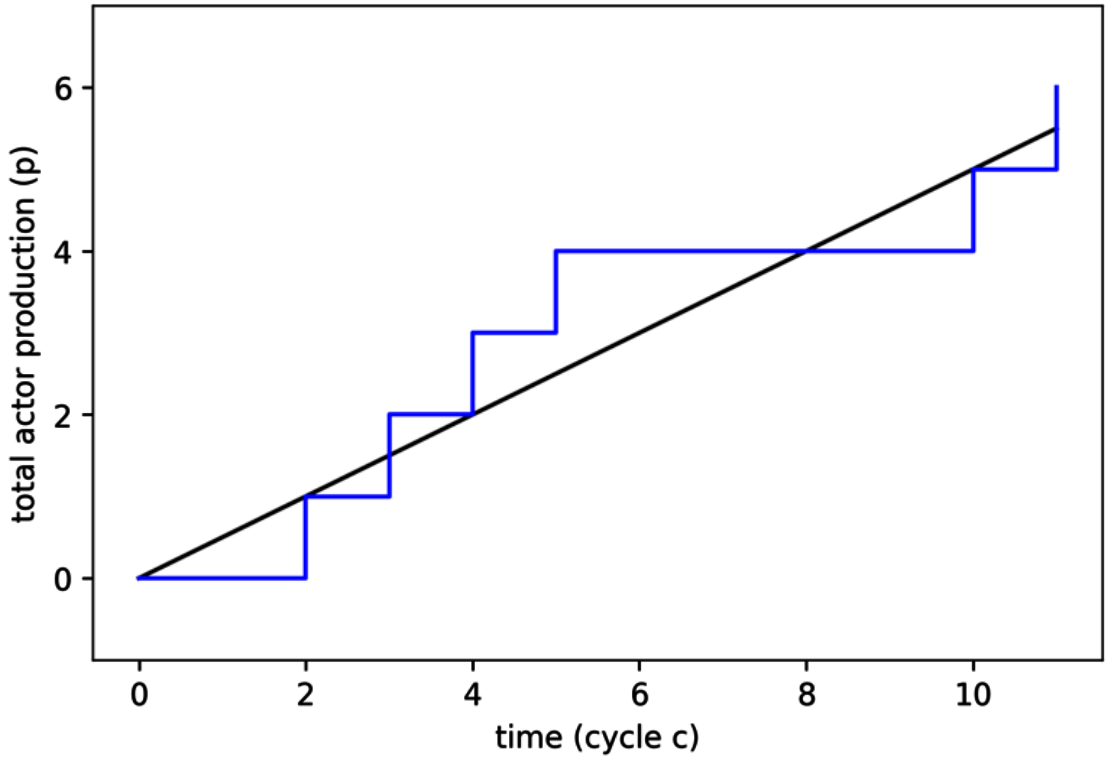

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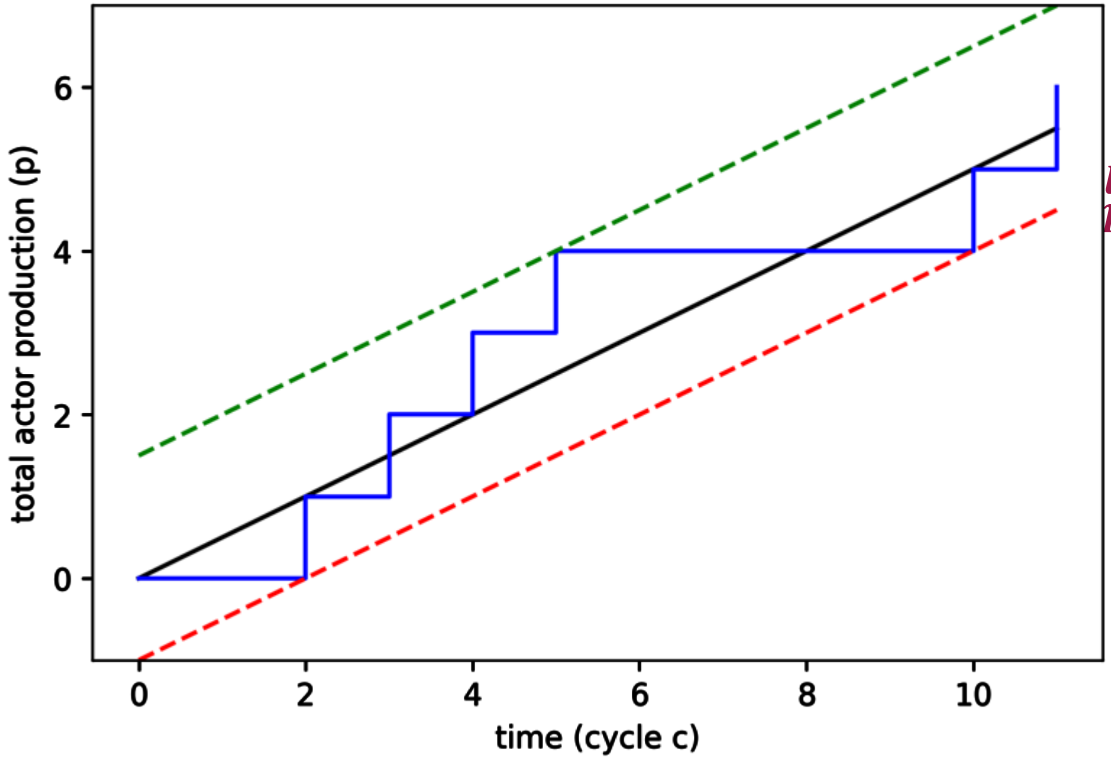
$cc-\ \lambda\ p\ l\ \lambda\lambda\ \lambda\ p\ l\ pp\ \lambda\ p\ l\ ll\ \lambda\ p\ l$
$\leq pp\ c\ cc\ c \leq a\ p\ aa\ a\ p\ pp\ a\ p$
$\times cc+\ \lambda\ p\ u\ \lambda\lambda\ \lambda\ p\ u\ pp\ \lambda\ p\ u\ uu\ \lambda$
$p\ u$
$\mathbf{11}$



${}_p^l \leq p(c) \leq$

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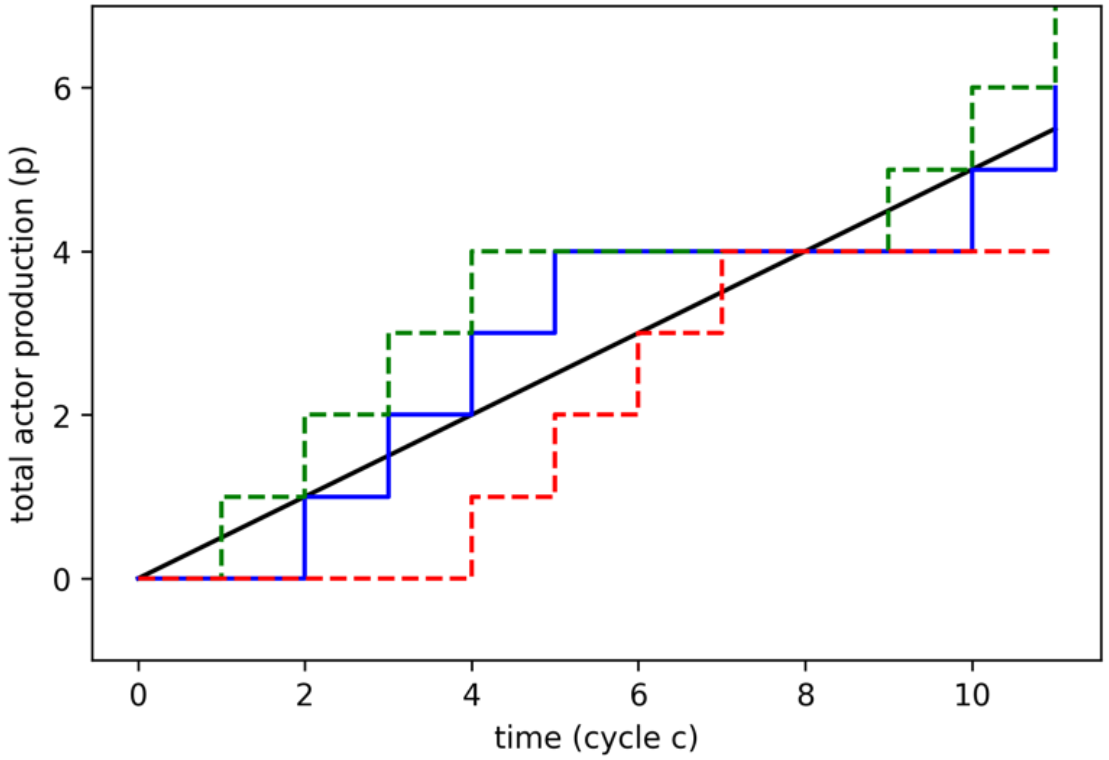

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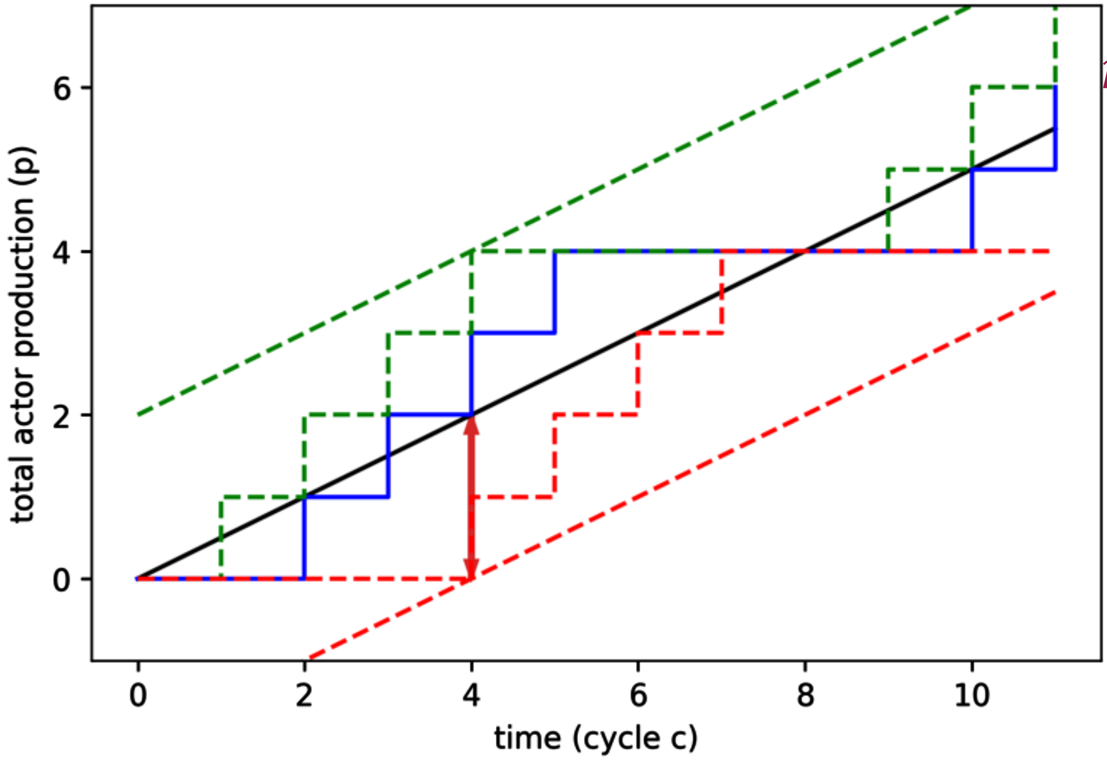
$\tau\ p\ c - \lambda p \leq p\ c \leq a\ p \times c + \lambda p$

$p\ p\ p\ p\ p\ \ p\ p\ \ p\ pp\ \tau\ p\ \ 1-\ \ \tau\ p$
$II\ \ 11-\ \ \tau\ p\ \ II\ \ \tau\ p\ \tau\tau\ \tau\ p\ pp\ \tau\ p$
$\tau\ p\ \ II\ IIII\ \ \tau\ p\ \ II\ \ 1-\ \ \tau\ p\ \ II$

Bounds:

$p \leq p(c) \leq$



Periodic scheduling

ILP constraints:

- **: FIFO size**
- **θ: delays**
- **φ: phase**

Fast for ILP formulation (3 variables per edge)

Guarantee optimal throughput (no push back by overflow)

Affine scheduling

Periodic scheduling

$$(1)\quad \theta_{e_{p\to c}} + a_p \frac{\varphi_{p\to c}}{n} \geq \lambda_c^u + \lambda_p^l + a_p C_{under}$$

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ILP constraints:

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2. Overflow
3. Cycles

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$$\frac{n}{d} = \frac{\tau_p}{II_p} \times \frac{II_c}{\tau_c}$$

$$(3)\quad \sum_{i=1}^{k} \left(\prod_{l=1}^{i-1} d_l \right) \left(\prod_{l=i+1}^{k} n_l \right) \varphi_i = 0$$

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Formally proven (A. Bouakaz thesis)

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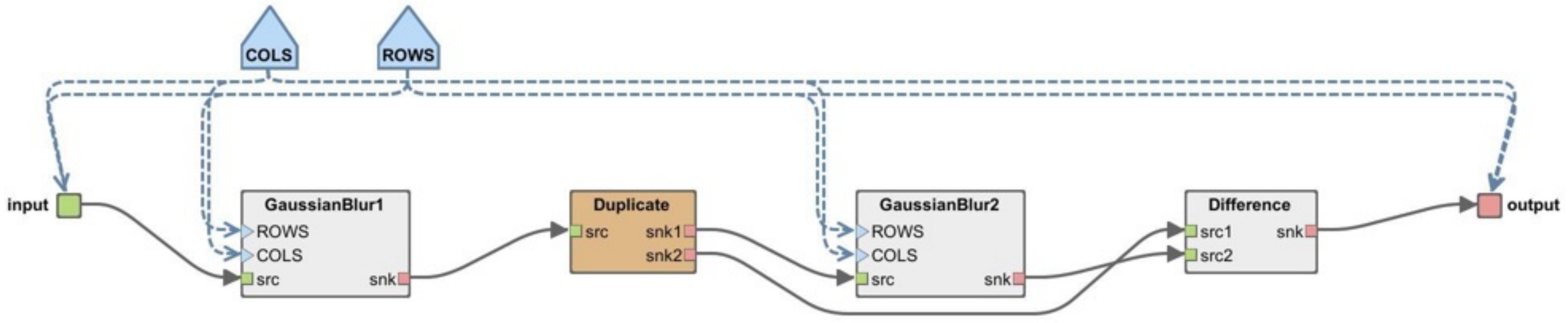
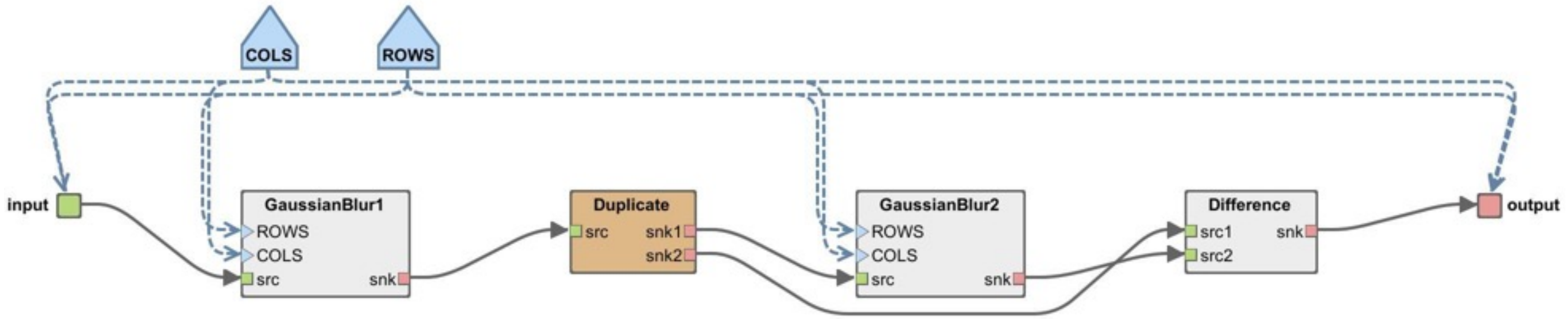
EXPERIMENTAL RESULTS

Gaussian Difference



[Undirected cycle]

Gaussian Difference

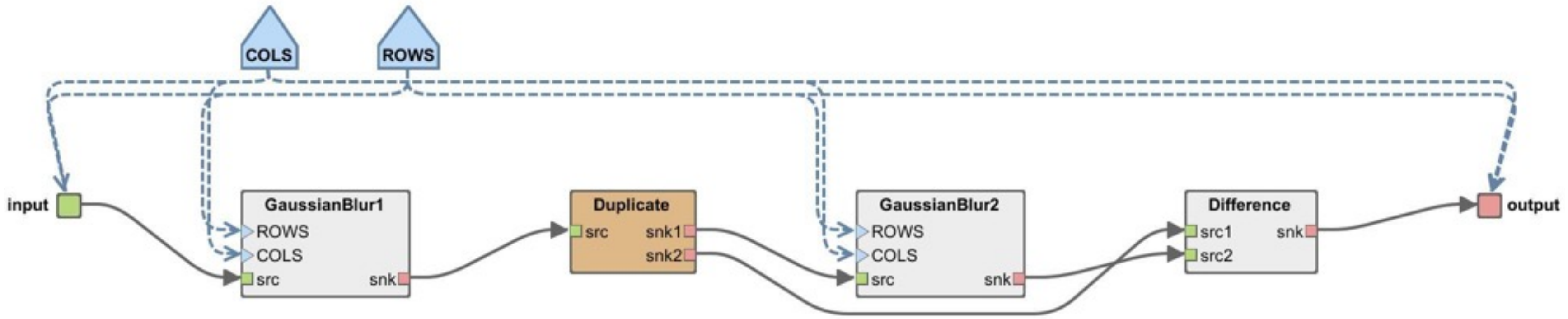


[Undirected cycle]

Setup:

- **Vitis Library kernels + graph**
- **PREESM computed FIFO sizes**

Gaussian Difference



[Undirected cycle]

Setup:

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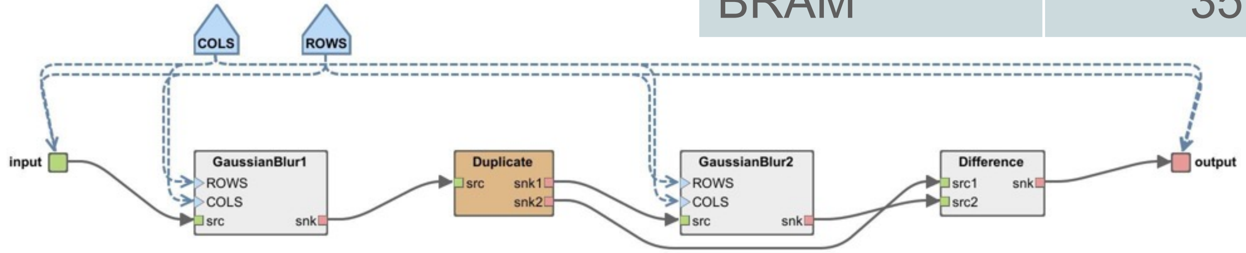
	Vitis Library	PREESM
[Undirected cycle]	15360	8580
[FIFO]	2	1276 - 7022
BRAM	18	35 (+49%)
Latency (Synthesis)	19914	19914
Latency (Cosimulation)	20870	19827 (-5%)

Gaussian Difference

- Reduce kernel latency

	Vitis + FIFO	PREESM
[Undir. cycle]	8580	2541
[FIFO]	1276 - 7022	2540
BRAM	35	12



Gaussian Difference

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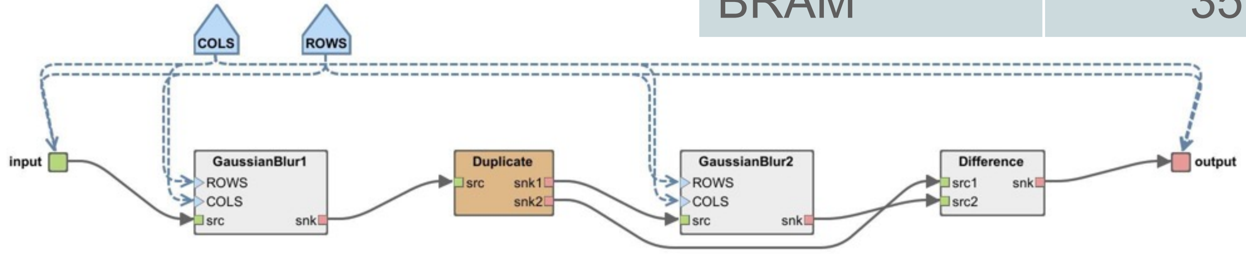
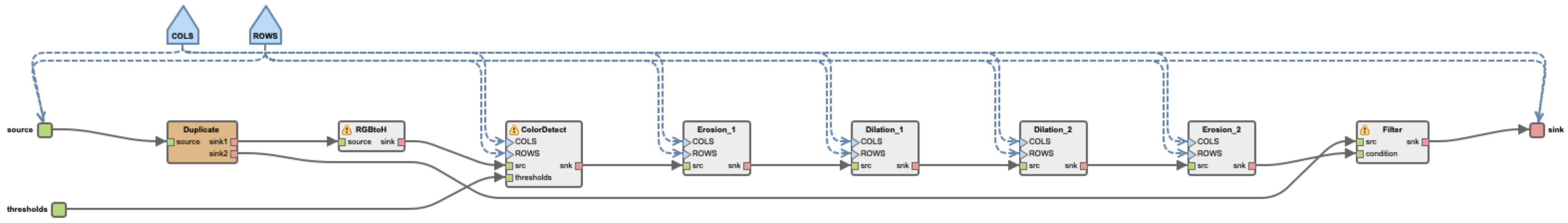


Color Filter

- **Move downsampling to small kernel**

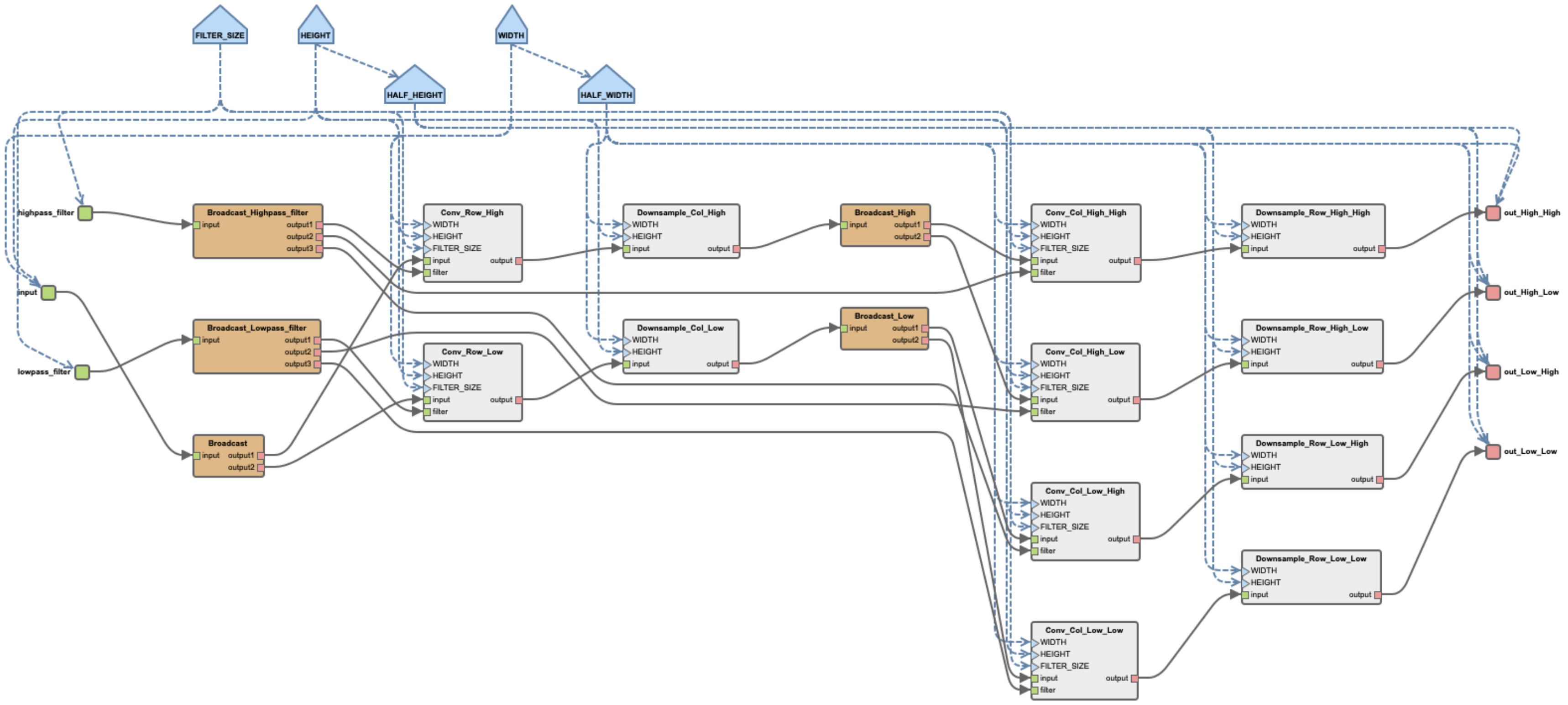
	PREESM	Optimized
[Undir. cycle]	808011	38002
[FIFO]	2 - 520936	2 - 5082
BRAM	790	61



2D Wavelet Transform

- **Reduce actor granularity**

	PREESM	Optimized
[FIFO]	12 - 50897	12 - 1510
BRAM	368	108



CONCLUSION

Contributions

- Dataflow code generation for FPGA using HLS
- Automatic scheduling and buffer sizing
- Open source implementation in PREESM

https://preesm.github.io

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- Improve buffer sizing
    - Data dependency
    - Actor internal scheduling

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    - Mapping + Scheduling + Code generation

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  - Data dependency
  - Actor internal scheduling
- Target heterogeneous platform
  - FPGA + CPU
  - Mapping + Scheduling + Code generation
- Design Space Exploration
  - Constraints based optimization
  - Memory optimization

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