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Dataflow code generation for FPGA

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High-level synthesis tools for FPGA such as Vitis HLS simplify the development of accelerated applications using high-level C language and combining pre-existing kernels. However connection of dataflow buffers between these kernels still need to be specified and optimized manually by the developer. In this presentation, we introduce a new method and associated tool to generate HLS code from a dataflow graph, and automatically compute buffer sizes to reach the highest throughput.

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