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Compiling circuits with polyhedra

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Hardware accelerators are unavoidable to improve the performance of computers with a bounded energy budget. In particular, FPGA allow building dedicated circuits from a gate-level description, allowing a very advanced level of optimization. Tools for high-level synthesis (HLS) allow the programmer to program FPGA without the constraints linked to hardware, compiling a C specification into a circuit. Code optimizations in these tools remain rudimentary (loop unrolling, pipelining, etc.), and most often the responsibility of the programmer. Polyhedral model, born from research on systolic circuits, offer a powerful tool to optimize compute kernels for HPC. In this seminar, I will show a few interconnections between HLS and the polyhedral model, either as a preprocessing (source-to-source) step, or as a synthesis tool (optimizing the circuit using a dataflow intermediate representation). In particular, I will present a dataflow formalism that allow reasoning geometrically on circuit synthesis.

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